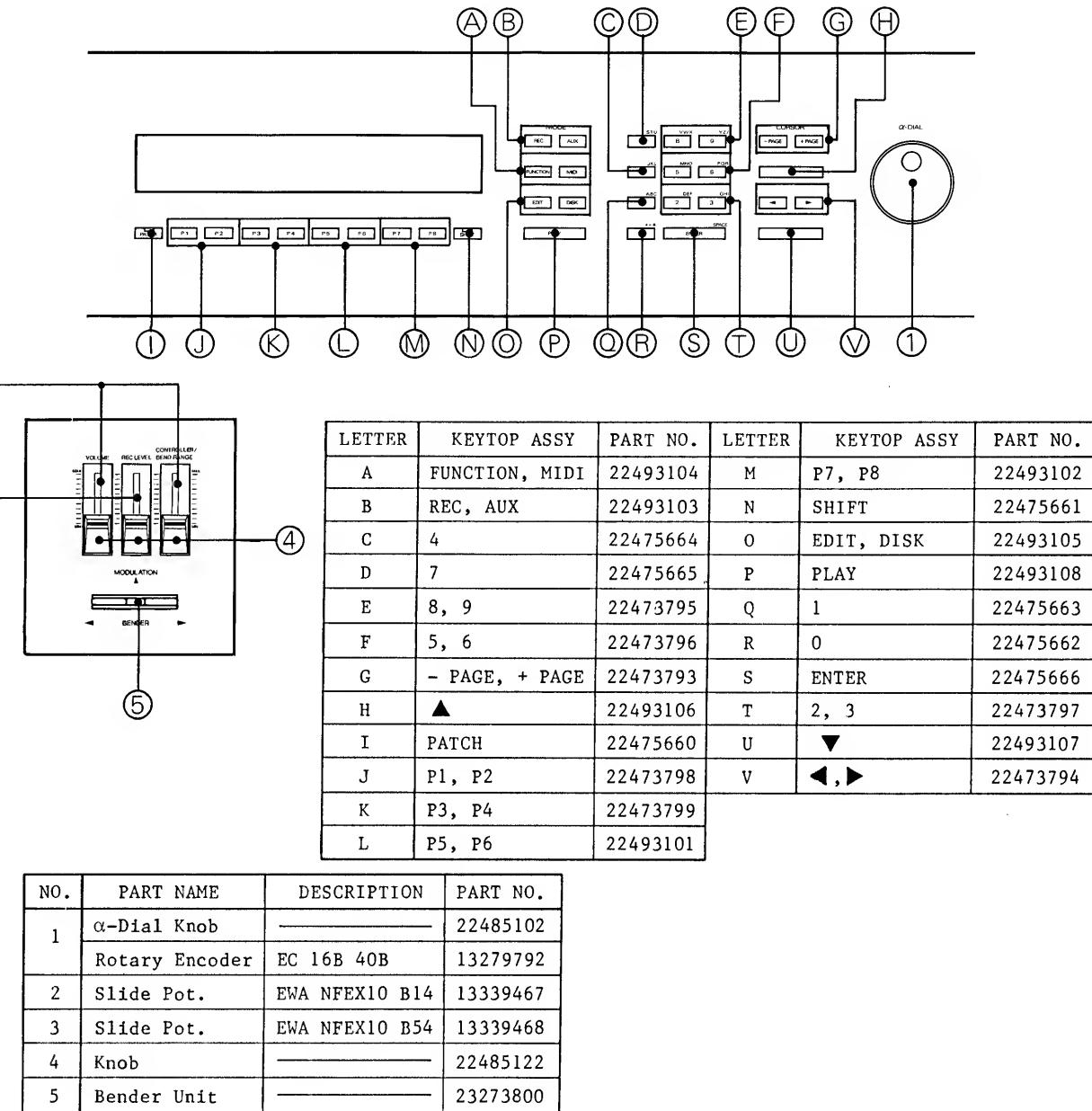
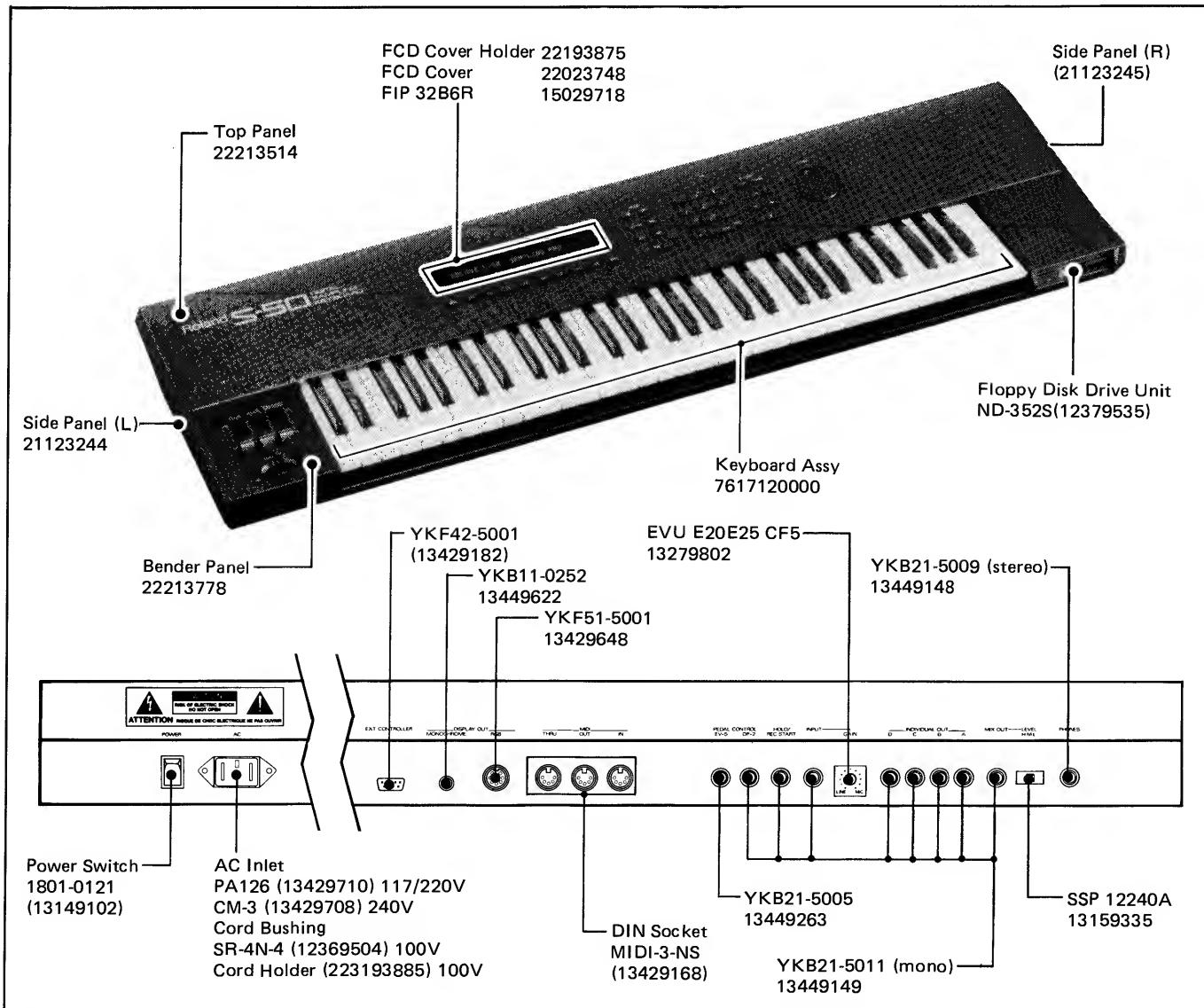


S-50

SERVICE NOTES *First Edition*

## SPECIFICATIONS

Keyboard	61 Key (C to C)	HOLD/REC START	OFF - 0V ; ON - 5V
Memory Capacity	a. Patch x8 b. Tones x16 (Bank A - 8 Tones, Bank B - 8 Tones)	CONTROL DP-2	OFF - 0V ; ON - 5V
Memory System	3.5 inch 2DD (double sided, double density, double track)	PEDAL EV-5	0V - 5V
AUDIO IN	Micro Floppy Disk Level -59dBm (MIC) to +4dBm (LINE)	DISPLAY OUT	RGB TTL level Horizontal Freq. 15.75KHz MONOCHROME COMPOSITE 1Vp-p
	Impedance 1.8KΩ (MIC) to 150KΩ (LINE)	EXT CONTROLLER	TTL level
OUTPUT	MIX OUT H = +10dBm max/3.3KΩ M = -4dBm max/10KΩ L = -20dBm max/4.6KΩ	Dimensions	1,106 (W) x 328 (D) x 93 (H) mm 43-7/16 x 12-15/16 x 3-11/16 in.
	INDIVIDUAL OUT A = +1.5dBm max/0.8KΩ B = +2dBm max/1KΩ C = +3dBm max/1.6KΩ D = +6dBm max/3.3KΩ	Weight	13 kg/28 lb. 11 oz.
	PHONES 20mW/8Ω	Power Consumption	36W
		Accessories	Connection Cord x 1 3.5 inch Floppy Disk x 5 Floppy Disk Case Owner's manual Instructions on CRT Guide Book "MIDI"
		OPTIONS	Pedal Switch : DP-2 Digitizer : DT-100 Expression Pedal EV-5 Carrying Case RGB Connection Cable : RGB 25I For 9 pin sub RGB Connection Cable : RGB 25N For 8 pin square



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**CAUTION**

Terminal lugs (battery terminal) on the bottom of CPU and Jack board serve as ground paths of magnetic shield circuit preventing EMI. Restore them in place if removed.

Please check for change information on page 8.  
There are some important design changes.

**注意事項**

- CPUボード及びジャックボードの裏面に取り付けてある端子は、EMI 対策用です。(電磁シールドのアース)  
取り外した場合は必ず元通りに取り付け直して下さい。
- 重要な変更についての案内を8頁に掲載していますので、必ず参照して下さい。

**PARTS LIST****PANEL, CASING**

22213514	Top Panel	
22213778	Bender Panel	
22813554	Chassis	
21123244	Side Panel (LEFT)	
21123245	Side Panel (RIGHT)	
22215771	DD Panel	

**KNOB, BUTTON**

22485122	Knob	(VOLUME, REC LEVEL, CONTROLLER/BEND RANGE)
22485102	Knob	(dial)
22475660	Button 247-660	(PATCH)
22475661	Button 247-661	(SHIFT)
22475662	Button 247-662	(0)
22475663	Button 247-663	(1)
22475664	Button 247-664	(4)
22475665	Button 247-665	(7)
22475666	Button 247-666	(ENTER)
22473793	Button 247-793	(-PAGE +PAGE)
22473794	Button 247-794	(◀ ▶)
22473795	Button 247-795	(8, 9)
22473796	Button 247-796	(5, 6)
22473797	Button 247-797	(2, 3)
22473798	Button 247-798	(P1, P2)
22473799	Button 247-799	(P3, P4)
22493101	Button 249-101	(P5, P6)
22493102	Button 249-102	(P7, P8)
22493103	Button 249-103	(REC, AUX)
22493104	Button 249-104	(FUNCTION, MIDI)
22493105	Button 249-105	(EDIT, DISK)
22493106	Button 249-106	(▲)
22493107	Button 249-107	(▼)
22493108	Button 249-108	(PLAY)

**SWITCH**

13149102	1801-0121	(Power)
13159335	SSP 12240A	(Slide)
13169633	SKH HAD 039A	(Tact)
13279792	EC 16B 40B	(Rotary Encoder, dial)

**JACK, SOCKET**

13429710	AC Inlet PA-126	(117/220V)
13429708	AC Inlet CM-3	(240V)
13449148	YKB21-5009	(Stereo) [Headphone]
13449149	YKB21-5011	(Mono) [Output, Pedal]
13449263	YKB21-5005	(Stereo with SW.) [Pedal Control (EV-5)]
13429168	MIDI 3-NS	(5P DIN, Triplet) [MIDI IN, OUT, THRU]
13429167J0	DBLC-J25SAF-22L8	(25P, D-Sub)
13429648	YKF51-5001	(8P DIN for RGB OUT)
13449622	YKB11-0252	(Pin Jack for Monochrome OUT)
13429182	YKF42-5001	(9P D-Sub for AUX Input Connector)

**POWER TRANSFORMER**

22453455U0	245-455U0	(100/220/240V)
22453465U0	245-465U0	(100/117/220/240V)

**COIL**

12449251	244-251	(for FIP driver)
12449244	SC-02-15E	(Line Filter)

**RESONATOR**

12389744	HC 49/U	8MHz	(Crystal)
12389758	HC 49/U	14.3496MHz	(Crystal)
12389759	HC 49/U	24MHz	(Crystal)
12389760	HC 49/U	26.880MHz	(Crystal)
12389748	CSB 600P	600KHz	(Cerelock)

**PCB ASSY**

7617110000	CPU board	(pcb 22923344)
7617109000	Jack board	(pcb 22923343)
7617113000	Power Supply board	(pcb 22923340)
7617108000	Volume board	(pcb 22923341)
7617115000	Panel board	(pcb 22923342)
7617112200	Filter board	100/117V (pcb 22923369)
7617112400	Filter board	220V (pcb 22923369)
7617112500	Filter board	240V (pcb 22923369)

**POTENTIOMETER**

13339467	EWA-NFEX10 B14	(Slide)
13339468	EWA-NFEX10 B54	(Slide)
13279802	EVU-E20E25 CF5	(Rotary, Input Gain)
13299193	EVN-D4AA00 B54	(Trimmer, CPU board)
13299201	EVN-D4AA00 B53	(Trimmer, Power Supply board)

**IC**

15179246	i8095-90	(CPU)
15219173	TMS 3556NL	(Video Display Processor)
15219171	EHK-MD6209	(D/A Converter)
15179343	HM6116ASP-12	(C-MOS S-RAM)
15179364	TMS4464-15NL	(64 x 4 D-RAM)
15179775	EP-ROM 27128	
15179374B0	M5M5256P-12	(32 x 8 S-RAM)
15179365	M5M4256L-12	(256k D-RAM)
15229830	MB63H149PF-G-BND	(Gate Array)
15229840	RF5C36	(Gate Array)
15229846	μPD65006CW-071	(Gate Array)
15219160	WD1770-00	(Floppy Disk Controller)
or 15219158 WD1772-02		
15169514B0	M74HC04P	(C-MOS Hex Inverter)
15159113H0	HD14051BP	(8-Channel Analog Multiplexer)
15169544N0	μPD74HC573C	(Octal Noninverting D-Type Latch)
15169515B0	M74HC00P	(2-Input NAND)
15169548B0	M74HC14P	(Hex Schmitt Trigger Inverter)
15169549N0	μPD74HC32C	(2-Input OR)
15169550B0	M74HC138P	(1-of-8 Decoder)
15169552B0	M74HC245P	(Octal 3-State Noninverting Bus Transceiver)
15169556N0	μPD74HC574C	(Octal 3-State Noninverting D-Flip-Flop)
15169555B0	M74HC393P	(Dual 4-State Binary Ripple Counter)
15169513B0	M74HC74P	(Dual D-Type Flip-Flop)
15169340B0	M74LS374	(Octal 3-State Noninverting D-Flip-Flop)
15179240	μPD7538 A-013	(CPU on Panel board)
15219159	μPD6300C	(FIP Latch Driver)
15229836	NJU7302	(Sample & Hold)
15189150	M5220L	(OP Amp)
15189193	M5238P	(OP Amp)
15199109N0	μPC78L05	(+5V Regulator)
15189158	μPC4082C	(OP Amp)
15199118N0	μPC7815H	(+15V Regulator)
15199102N0	μPC7915	(-15V Regulator)
15199106NH	μPC7805H	(+5V Regulator)
15189186	μPC4570C	(OP Amp)
15189111P0	IR-9311	(Comparator)
15219174	NJU201AD	(Analog SW.)

TRANSISTOR	
15119108	2SA798C
15129602	2SD667C
15119602	2SB647C
15119601	2SB605L
15129606	2SD84Y
15129615	2SD1293M
15119106	2SA730Q
15129150	DTCL114F
15129107	2SC945Q
15129136	2SC2878

DIODE, LED, PHOTO COUPLER	
15019125	1SS-133
15019208	1SR35-200A
152370650	PC-55VC 3F (Photo Coupler)
15029222	SC-55VC 3F (LED)
15019243	1BA1
15019274	D5TB-20 (Rectifier)
15019503	05Z 9.1Z (Zener)
15019143	1S-116
15029718	FIP32B6R (Fluorescent Indicator Panel)

RESISTOR	
13919147	RMLS 4-103J (10k x 4)
13919312	RMLS 8-103J (10k x 8)
13919312	RMLS 8-153J (15k x 8)
13919313	RMLS 8-104J (100k x 8)
13919118R0	RKM 10L 104F (Ladder Network)
13919336	RMLS 8-224J (220k x 8)
13919168	RMLS 4-224J (220k x 4)
13919322	RMLS 4-102J (1k x 4)

CAPACITOR	
13529104	DE7150F472MVA1 (Line Capacitor)
13529108	RPE132F104Z50V (Ceramic 0.1μ)
13529113	EXFP8101MW (100P x 8)
13529118	B72C0724-32N (22P x 6)
13529118	B5RC0139 (22P x 4)

FUSE, FUSEHOLDER	
12559509	SD6 630mA (100/117V)
12559510	CEE-400mAAT (220/240W)
12199552	UF0005-02 (Fuse Holder)

HOLDER	
22193886	Jack
22195889	MIDI Socket
22193875	FCD Cover (FIP Cover)
22193874	adial

AC CORD, CORD SET	
13439801	P-VFF 2.5m (100V)
12369504	Cord Bush SR-4N-4 (100V)
22193885	Cord Holder (100V)
13439812FO	UC704-J01 (117V)
13439813FO	EC210-J06 (220V)
13439814FO	SC415-J06 (240V 3P, Australian)
13439846	BH-301-J01 (240V 3P, England)

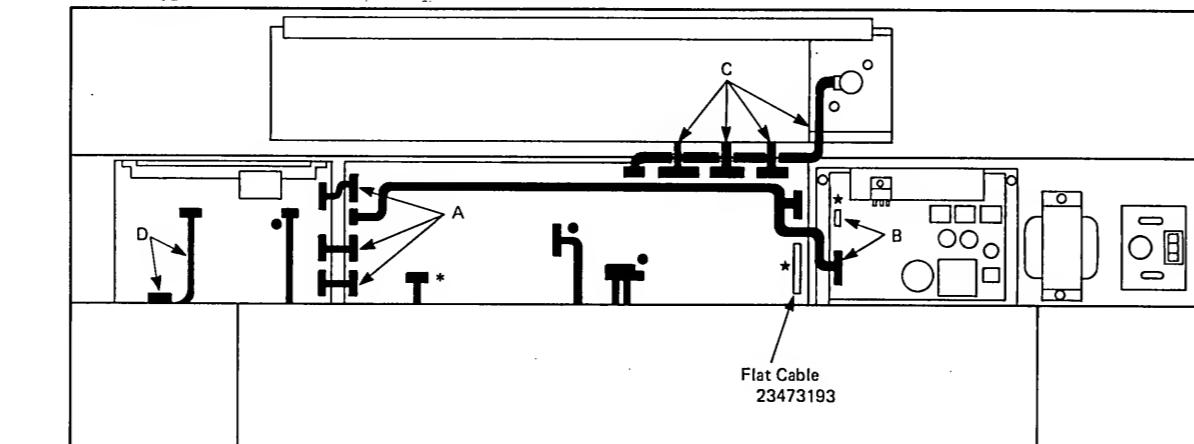
COVER	
22033748	FCD Cover (FIP Cover)
22033215	Connector Cover (25pin D-sub Connector)
22253126	Bender Shield Cover
22243150	Slide Cover
22245142	Mask (for adial)
22023318	Jack Shield Cover

CONNECTOR	
13439327	5267-02A
13439260	5267-03A
13439261	5267-04A
13439263	5267-06A
13439264	5267-07A
13439265	5267-08A
13439269	5267-09A
13439266	5267-10A
13439278	5267-11A
13439303	5566-06A

(Power Supply Board)

WIRING	
23493479	Wiring A
23493480	Wiring B
23493481	Wiring C
23493499	Wiring D
23473193	Flat Cable 347-193 (CPU Board - Disk Drive Unit)

WIRING



A : Wiring A 23493479 \* : to Floppy Disk Drive Unit  
 B : Wiring B 23493480 \* : to Bender Unit  
 C : Wiring C 23493481 \* : to Keyboard Assy  
 D : Wiring D 23493499

FLOPPY DISK SYSTEM

22373539	SYSTEM DISK (Set of 5 pcs)
12379535	Floppy Disk Drive Unit FDD4261 ACK
22163542	FDD Spacer
22263382	FDD Cushion
22013196	Floppy Disk Case

KEYBOARD ASSY

7617120000	Keyboard Assy
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LC FILTER	
22445281	TFB-3 (FC=12.5kHz)
22445282	TFB-3 (FC=13.5kHz)

OTHERS	
12199569	Locking Card Spacer KCLS-12R (Black)
12359105	Rubber Foot
23273800	Bender Unit PB-17
12439217	Relay NL6Y-DC5V
12449266	Ferrite Beads Inductor BLO1RN1-A62 (EMI Filter)
13529140	EMI Filter DSS310-55B271M
13429523	IC Socket SMO-28-567
No Code	Scale (Input Gain)
22123552	Angle
22123563	Shield Angle
12469139	Heat Sink 16PC16
22463149	Heat Sink 246-149 (for 2SD844)

## PANEL DISASSEMBLY

1. Remove Screws A. (Fig. 1)

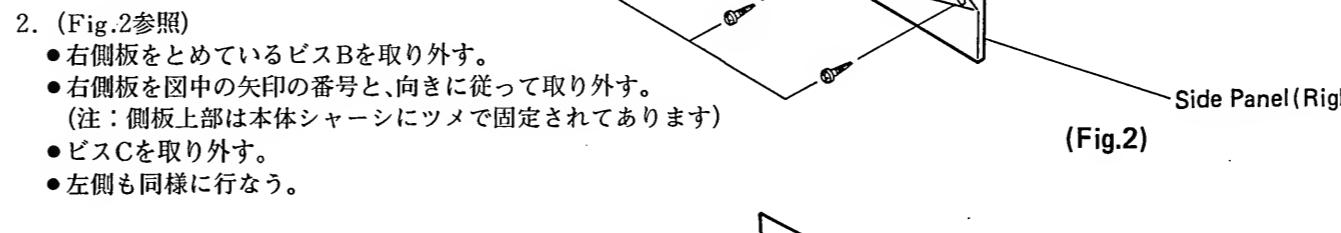
トップパネルの開け方  
 1. (Fig.1参照)  
 ●ビスAを取り外す。



(Fig.1)

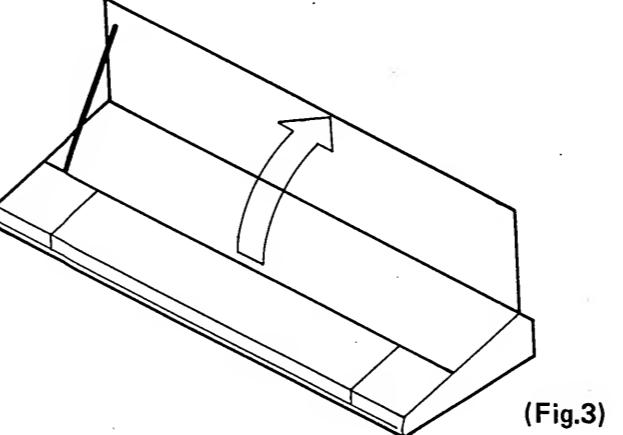
2. Remove Screws B from the right side panel. (Fig. 2)

● Grasp the top of side panel.  
 ● Note that the side panel has 3 "snap locks" inside.  
 ● Pull the side panel in a direction as shown by arrows 1 and 2 in Fig. 2.  
 ● Remove Screws C.



(Fig.2)

2. (Fig.2参照)  
 ●右側板をとめているビスBを取り外す。  
 ●右側板を図中の矢印の番号と向きに従って取り外す。  
 (注:側板上部は本体シャーシにツメで固定されています)  
 ●ビスCを取り外す。  
 ●左側も同様に行なう。



(Fig.3)

## KEYBOARD DISASSEMBLY

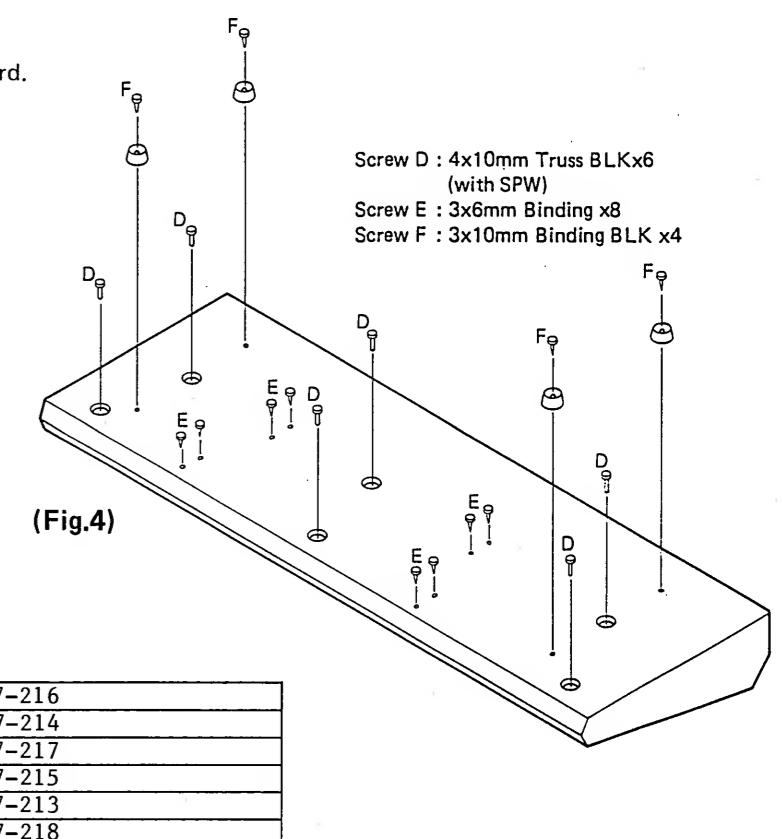
1. Open the top panel and then remove the CPU board.

2. Remove screws D and E in Fig. 4.

## 鍵盤の取り外し方

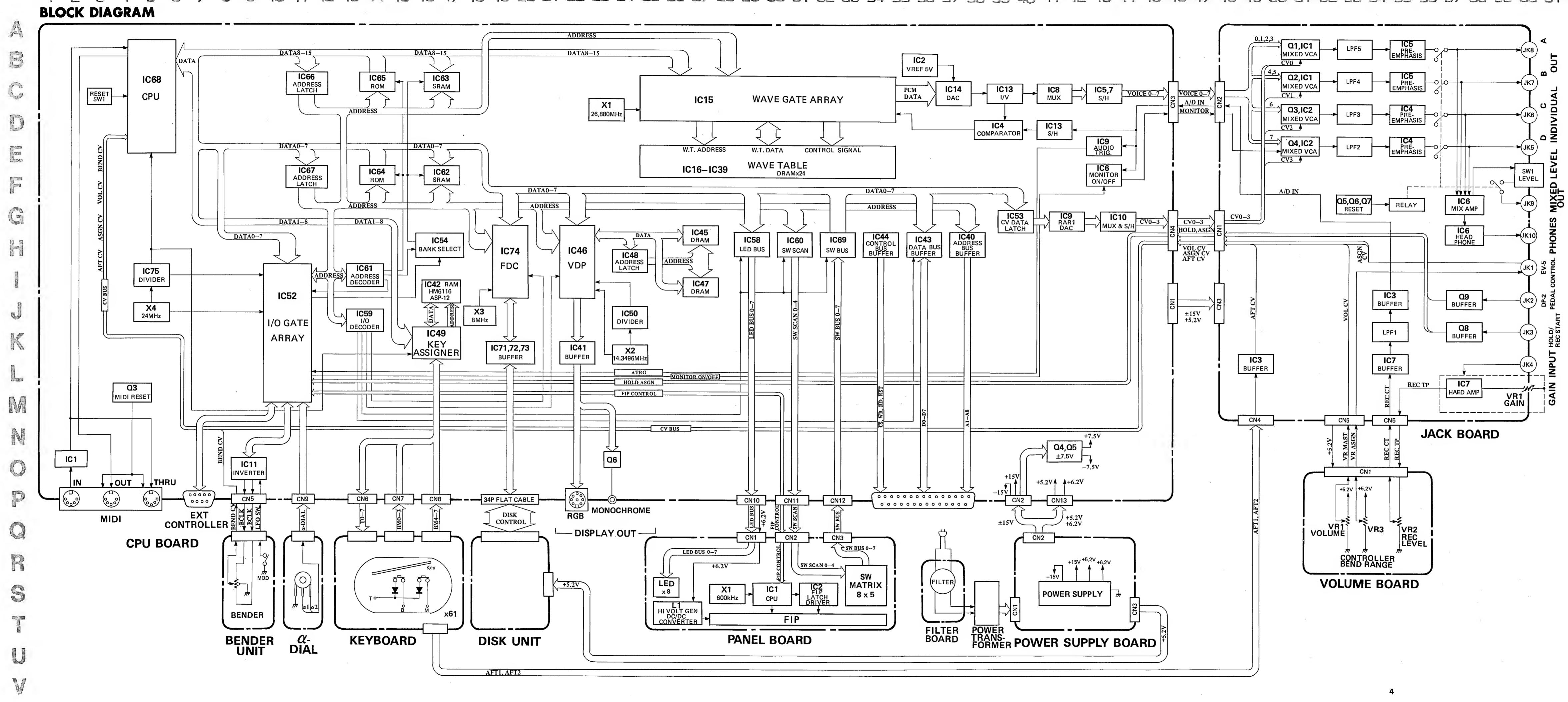
1. トップパネルを開け、CPUボードを取り外す。

2. Fig.4のD及びEのビスを取り外す。

KEYBOARD PARTS  
SK-361-OW
①	22575216	NATURAL KEY C,F	257-216




<tbl\_r cells="



## CIRCUIT DESCRIPTIONS

### General

The S-50 is a 16-voice sampling keyboard consisting of the following major sections.

### Control Section

CPU 8095 (IC68) having a 16 bit data bus. Controls the following function and the chips.

- Transfer of MIDI messages

- Wave Gate Array RF5C36

- Keyboard Gate Array MB63H149

- Keyboard Assigner Gate Array MB63H149

- Floppy Disk Controller (FDC) WD1770

- Video Display Processor (VDP) TMS3556

- FIP CPU  $\mu$ PD7538A

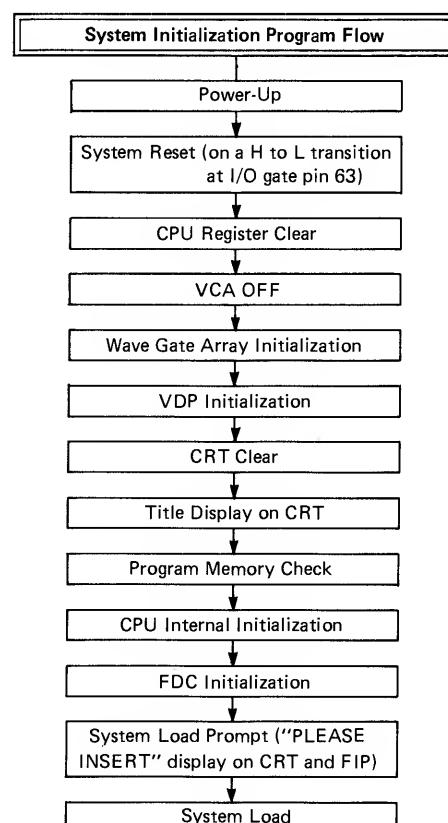
### Waveform Storage Section

Manages storage of the sound in the 24 256k-bit DRAMs through wave gate array RF5C36.

### System Operations

#### Software

The internal ROM program contains the initial setup and the basic subroutines. Figure 1 shows the program flow diagram. The system program is to be loaded from the disk.



(Fig.1)

## 回路解説

### 概要

S-50は、16ボイスのデジタル・サンプリング・キーボードで主な構成は次の通りです。

### 制御部

メインCPUには8095が使用されており、下記のものを制御しています。

- MIDIメッセージの送受信
- ウェーブ・ゲートアレイ RF5C36
- キーボード・アサイナ・ゲートアレイ MB63H149
- FDC [ フロッピー・ディスク・コントローラ ] WD1770
- VDP [ ビデオ・ディスプレイ・プロセッサ ] TMS3556
- FIP用CPU  $\mu$ PD7538A

### 波形記憶部

ウェーブ・ゲートアレイ RF5C36により、入力音の波形データを256KビットのDRAM 24個に記憶させています。

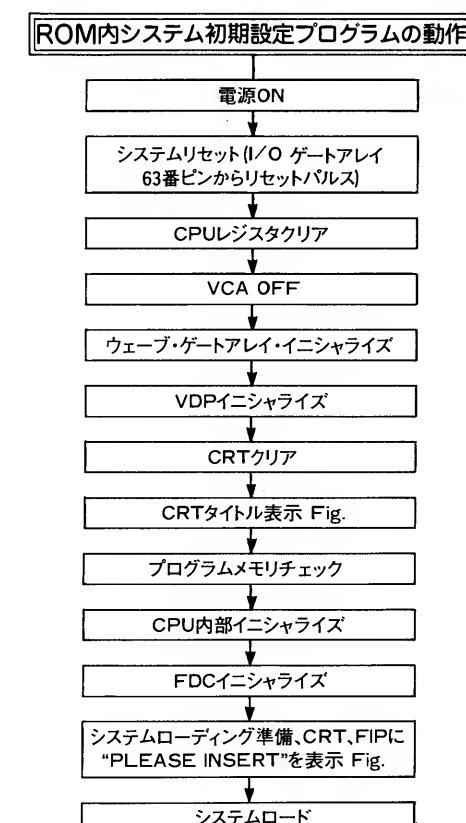
### 詳細

#### システム動作

##### ソフトウェアについて

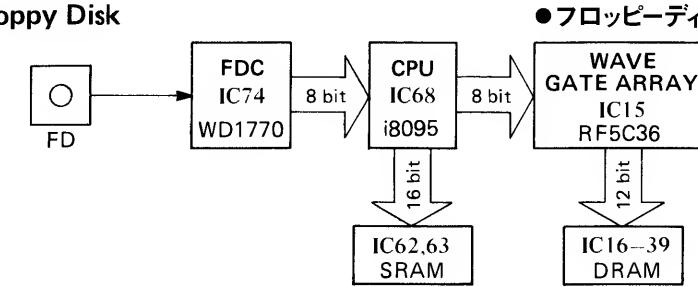
システムソフトウェアはディスクにより本体に供給されます。本体ROM内には、システムの初期設定プログラム及び基本サブルーチン等が格納されています。

ROMのシステム初期設定プログラムの流れをFig.1に示します。



(Fig.1)

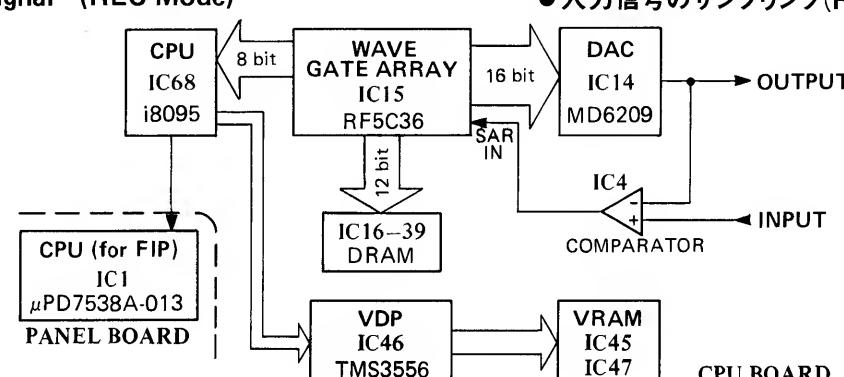
### Data From the Floppy Disk



CPU BOARD (Fig.2)

波形データは、DRAM (IC16~39)へ、システムプログラム及びその他のパラメータはSRAM (IC62, 63)へ格納されます。

### Input Sampling Signal (REC Mode)



CPU BOARD (Fig.3)

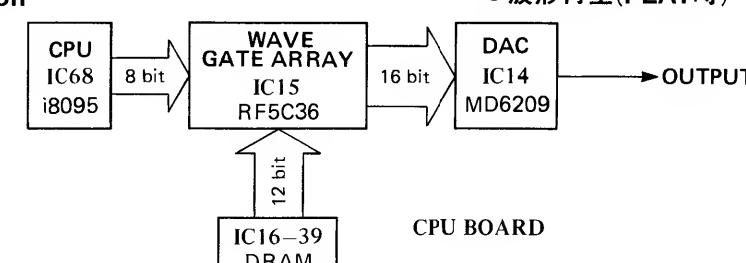
The A/D converter consisting of gate array (IC15), D/A converter (IC14) and comparator (IC4) converts the input signal into a digital data using the successive approximation method and stores the data into DRAMs (ICs 16~39).

The CPU monitors the input level in the IC15 and sends it to VRAMs (ICs 45 and 47) and FIP CPU (IC1) for use as level meter data.

### 入力信号のサンプリング(REC時)

ウェーブゲートアレイ (IC15)、D/Aコンバータ (IC14)、コンパレータ (IC4)で逐次比較型のA/Dコンバータを構成しています。入力信号はこのA/Dコンバータによりデジタルデータに変換され、DRAM (IC16~39)へ格納されます。CPU (IC68)はINPUTレベルを監視し、VRAM (IC45, 47)及びFIP用CPU (IC1)にレベルメータのデータを転送します。

### Waveform Reproduction



(Fig.4)

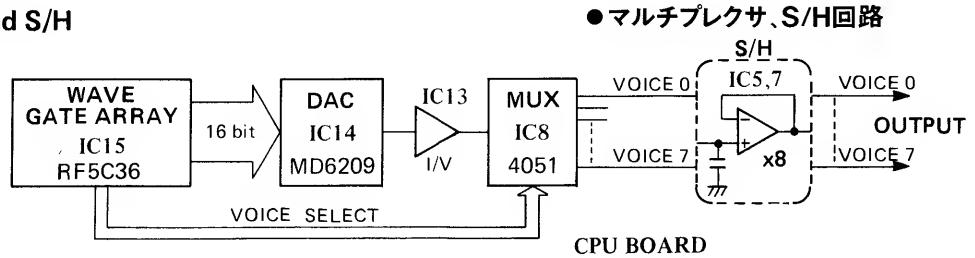
The CPU (IC63) sends the gate array (IC15) the information containing Note, Envelope, Loop concerning a sound to be played.

The gate array (IC15), upon receiving the data, reads the corresponding 12-bit wave data from DRAMs, processes the data with the envelope data to generate a 16-bit data and passes it onto the next stage, DAC (IC14).

### 波形再生(PLAY時)

CPU (IC68)はウェーブゲートアレイ (IC15)にNOTE情報、ENVELOPE、LOOPの各情報を送ります。ウェーブゲートアレイ (IC15)は前記のデータを受けとると、DRAMからの12bitデータをENVELOPE値との演算により16bitデータに変換し、DAC (IC14)へ送ります。

### ●Multiplexer and S/H

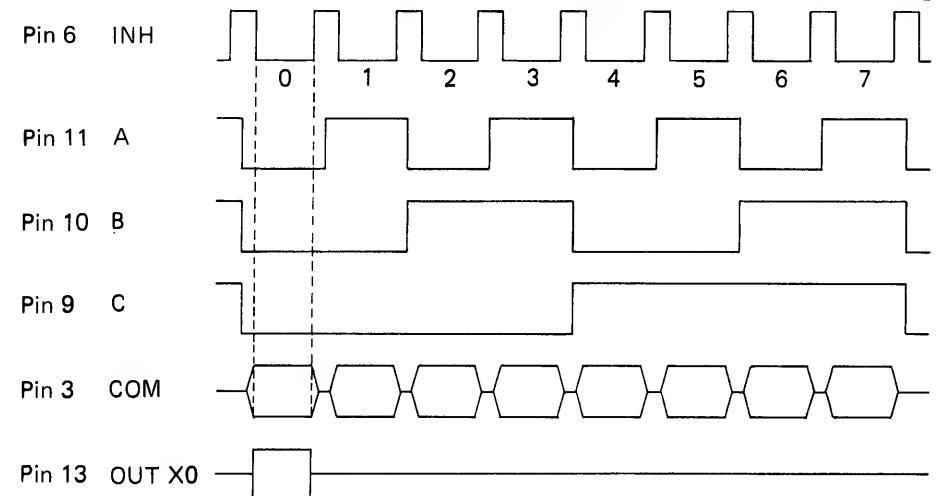


The DAC (IC14) splits 16 voices into 8 groups and outputs a set of 2 voices one by one in a timesharing fashion. Being a current producing type, its outputs are converted to voltage through I/V converter (IC13). The NUX (IC3) routes each 2-voice to the correct channel's S/H circuit. Shown below is the timing diagram of the MUX.

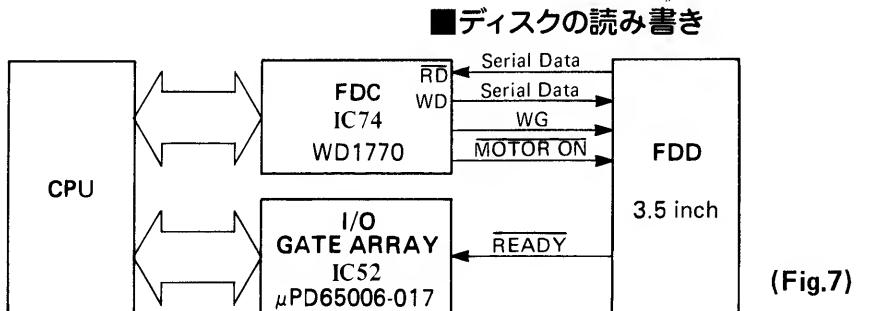
DAC (IC14) は、16 ボイスを 8 組に分け、2 ボイスづつをミックスして時分割で出力します。この出力は電流型であるため、I/V コンバータ (IC13) で電圧型に変換されます。

MUX (IC8) は、この時分割信号を 8 組に再分離し、S/H 回路へ送ります。

MUX のタイミングチャートを Fig. 6 に示します。



### ■Disk Read/Write



On a read or write command from the CPU, the FDC pulls MOTOR ON low to let the FDD (Floppy Disk Drive) starts the motor. When the motor running has reached stable condition, the FDD signals the CPU through I/O gate with a low READY. The low READY allows the CPU to issue a command which enables reading or writing to/from the disk.

In the read mode the FDC reads data from FDD in serial format and sends it to the CPU in parallel 8 bits.

In the write mode the FDC first pulls and keeps WG high and then places a data on WD line.

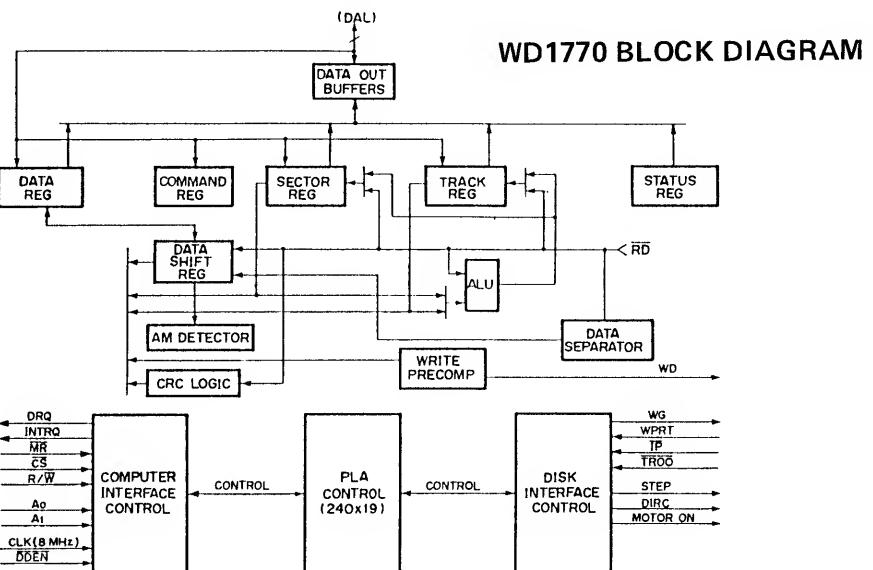
FDC は CPU からリード又はライトコマンドを受けると、FDD (フロッピーディスクドライブ) に対して MOTOR ON 信号を送り FDD のモーターを回転させます。

FDD はモーターの回転が安定すると、CPU に READY 信号を I/O ゲートアレイを介して送ります。

CPU は READY 信号を受けると読み込み又は書き込み動作を開始させます。

リード時、FDC は RD 端子より FDD からのシリアルデータを受けとり CPU に転送します。

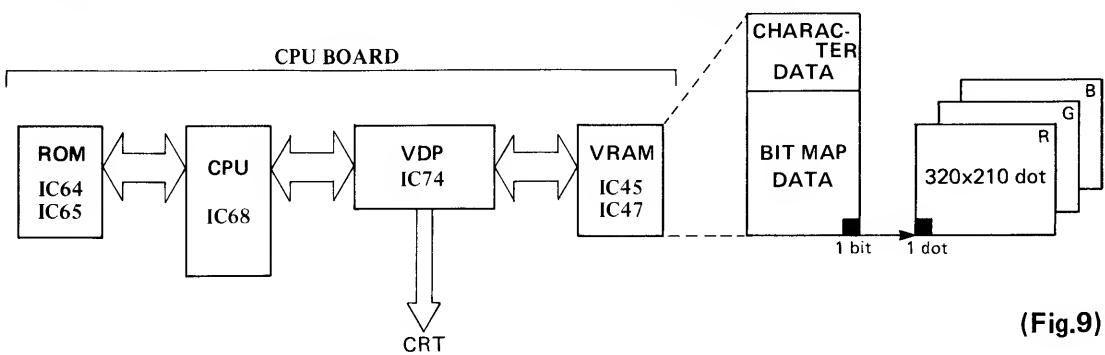
また、ライト時 FDC は WG 信号を High レベルにし、WD 端子を通じてデータを FDD に書き込みます。



FDC Pin Description

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
1	CS	CHIP SELECT	I	A logic low on this input selects the chip and enables Host communication with the device. Low LevelでCPUとのコミュニケーションが可能になります。
2	R/W	READ/WRITE	I	A logic high on this input controls the placement of data on the D0-D7 lines from a selected register. While a logic low causes a write operation to a selected register. リード・サイクルのときは High Level、ライト・サイクルのときは Low Level にします。
3, 4	A0, A1	ADDRESS 0, 1	I	These two inputs select a register to Read/Write data. 次に示すように、この2つの入力によってリード、またはライト・サイクルにおけるFDC内部のレジスタを選択します。
5-12	DAL0-DAL7	DATA ACCESS LINES 0 THROUGH 7	I/O	Eight-bit bi-directional bus used for transfer of data, control, or status. This bus is enabled by CS and R/W. Each line will drive one TTL load. 8ビットのデータ・バスで、データのやりとりに使用されます。
13	MR	MASTER RESET		A logic low pulse on this line resets the device and initializes the Status Register (internal pull-up). Low Levelで、FDCリセットします。
14	GND	GROUND	I	Ground. 電源グランドに接続します。
15	Vcc	POWER SUPPLY	I	+5V ±5% power supply input. +5V電源に接続します。
16	STEPP	STEP	O	The Step output contains a pulse for each step of the drive's R/W head. ディスク・ドライブのヘッドをHigh Levelでディスクの内側へ、Low Levelでディスクの外側へステップさせるための方向を設定します。
17	DIREC	DIRECTION	O	The Direction output is high when stepping in towards the center of the diskette, and low when stepping out. ディスク・ドライブのヘッドをHigh Levelでディスクの内側へ、Low Levelでディスクの外側へステップさせるための方向を設定します。
18	CLK	CLOCK	I	This input requires a free-running 50% duty cycle clock (for internal timing) at 8MHz ±0.1%. 8MHz ±0.1% 50%デューティサイクルのクロックを入力します。
19	RD	READ DATA	I	This active low input is the raw data line containing both clock and data pulses from the drive. ディスク・ドライブからデータを受けます。
20	MO	MOTOR ON	O	This active high output turns on the motor. ディスク・ドライブのモータを制御します。
21	WG	WRITE GATE	O	This output is made valid prior to writing on the disk. ディスク・データを書き込むときに High Levelになります。
22	WD	WRITE DATA	O	FM or MFM clock and data pulses are placed on this line to be written on the diskette. データをディスク・ドライブへ送ります。
23	TROO	TRACK 00	I	This active low input informs the WD1770-00 that the drive's R/W heads are positioned over Track zero (internal pull-up). トランク00信号を受けます。Low Levelのときはディスク・ドライブのヘッドがディスクの最も外側に位置します。
24	IP	INDEX PULSE	I	This active low input informs the WD1770-00 when the physical index hole has been encountered on the diskette (internal pull-up). インデックス信号を受けます。この信号はディスクが1回転するごとにディスク・ドライブから送られます。
25	WPRT	WRITE PROTECT	I	This input is sampled whenever a Write Command is received. A logic low on this line will prevent any Write Command from executing (internal pull-up). ライト・プロテクト信号を受けます。この信号は、ディスクにライト・プロテクトがかかっているときにディスク・ドライブから送られます。
26	DDEN	DOUBLE DENSITY ENABLE	I	This input pin selects either single (FM) or double (MFM) density. When DDEN=0, double density is selected (internal pull-up). High Levelで単密度(FM)に、Low Levelで倍密度(MFM)に設定されます。
27	DRQ	DATA REQUEST	O	This active high output indicates that the Data Register is full (on a Read) or empty (on a Write) operation. この出力の立ち上がりでデータ・レジスタがリードのときはフル、ライトのときはエンptyであることをCPUに知らせます。
28	INTRO	INTERRUPT REQUEST	O	This active high output is set at the completion of any command or reset at a read of the Status Register. この出力の立ち上がりで、コマンドの実行終了をCPUに知らせます。

■ Video Display Processor  
(VDP) TMS-3556



The figure 9 below shows the block diagram of the VDP, IC74 and associated circuits. The VDP operates either of TEXT and BIT MAP modes.

● Text Mode

In the text mode the CPU sends the VDP a character code and the coordinates of the character on the screen. The VDP fetches the character pattern data from the VRAM character area and displays the character in a 10 by 8 dot matrix on the 21 row by 40 character screen.

● Bit Map Mode

The VRAM bit map area is divided into three portions, each corresponds to color R, G, or B of 320 by 210 dot matrix on the screen. When in this mode, the CPU writes image data into the bit map area. The VDP displays pixel by pixel with specified color.

■ VDPビデオ・ディスプレイ・プロセッサ  
TMS3556

VDPの周辺ブロック図をFig. 9に示します。  
VDPは次の2種類のモードで動作しています。

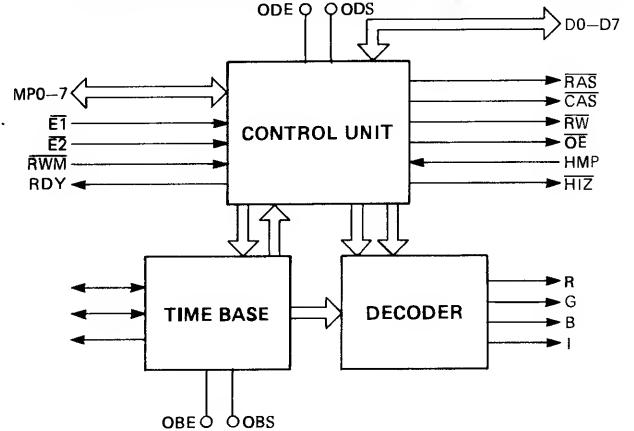
●テキストモード

CPUから表示する座標点データと文字コードを受け取ると、VRAM内部のキャラクタ領域から、キャラクタパターンを、読み込み41行×21行で表示します。

●ビットマップモード

画面を、R, G, B 3枚のシートに分解し、1シート(320×210ドット)の1ドットをVRAM内ビットマップ領域の1ビットに対応させて表示します。したがってCPUがVRAMのビットマップ領域へ画面データを書き込む事により、ドット毎に色を指定した各種グラフィック等を、描くことができます。

VDP TMS3556 BLOCK DIAGRAM (Fig.10)



■ I/O ゲートアレイμPD65006-017(IC52)

内部ブロック図をFig. 11に示します。  
ポート及びコントローラ等を内蔵しており各種コントロール信号の発生、αダイヤル及びディジタイザのインターフェイスの役割をします。

●ディジタイザ [EXT CONTROLLER] 用端子

ディジタイザ(DT-100)と同期式のシリアル伝送を行なうための端子です。  
各ピン端子機能についてTable 3に示します。

EXT CONTROLLER Pin Description (Table 3)

PIN NUMBER 端子番号	SYMBOL 記号	SIGNAL NAME 信号名	I/O	FUNCTION 機能
1	M×0	SENSE	I	Senses input on the digitizer pad. パネル入力検出信号
2	M×1	EOC (End of Conversion)	I	Indicates the end of an A/D conversion cycle. A/D変換の終了信号
3	M×2	SI	I	Serial data. シリアルデータ
4	M×3	SW	I	A low on this input is signaling that the stylus(switch) is on. スタイラスのSW入力信号をONになるとLowレベルになる。
5	+5.2V	+5.2V	/	+5.2V power supply. 電源+5.2V
6	M×4	SCK	O	Clock input. クロック入力
7	M×5	SO	O	Serial data. シリアルデータ
8	M×6	CS	O	A low CS enables communication with the digitizer. Lowレベル時にコミュニケーションが行なえます
9	GND	GND	/	GND グランド

■ I/O Gate Array μPD65006-017 (IC52)

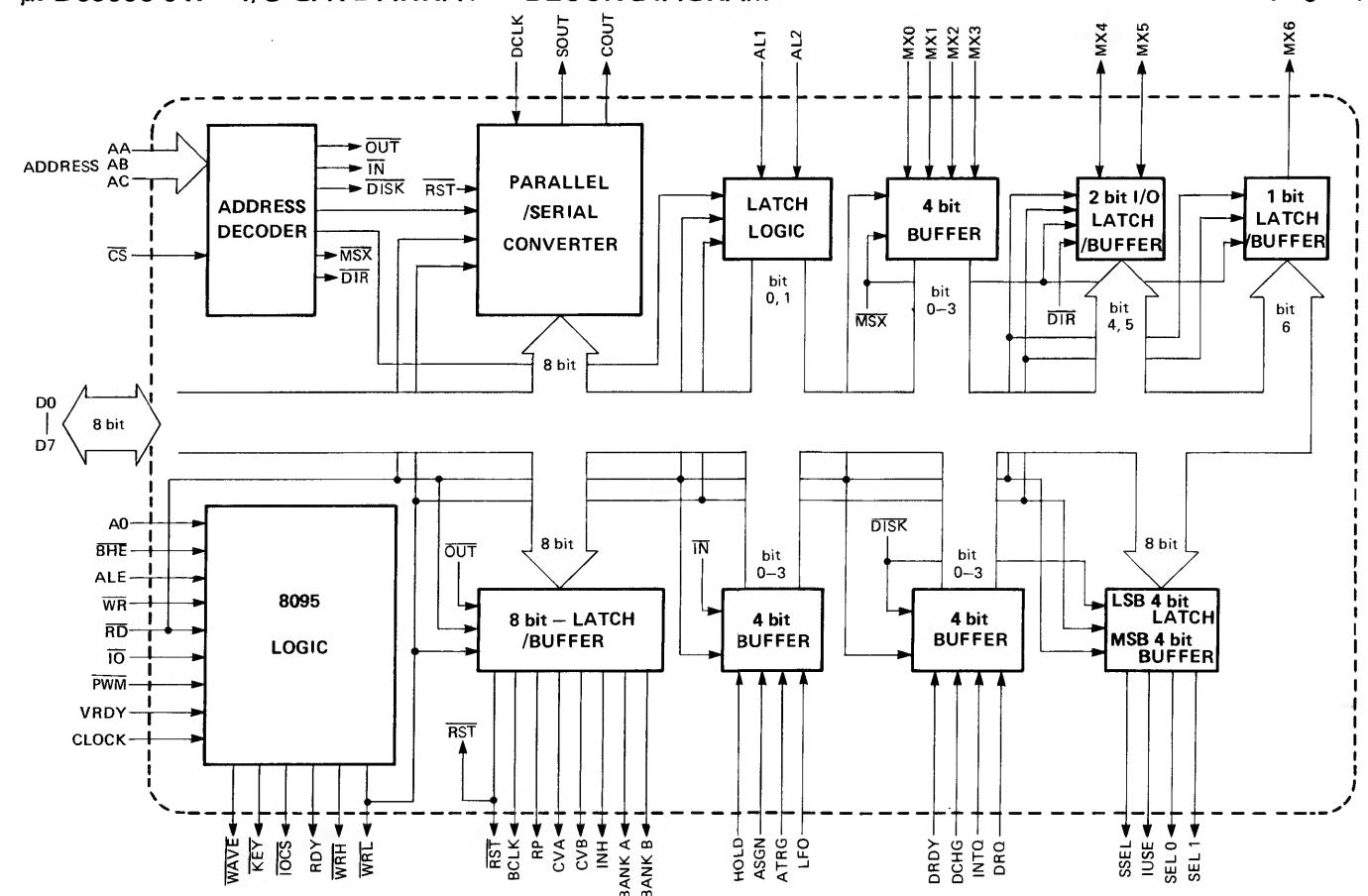
Figure 11 shows an internal block diagram of the Gate Array. The controller generates various control signals which determine the operational timings of most of the system stages.

The μPD65006-017, in addition to many I/O parts, has the ports for interfacing with α-dial and EXT controller.

● EXT CONTROLLER Socket

This socket enables communications with a digitizer (e.g. DT-100) in synchronous serial format. The pin assignment is as shown below.

μPD65006-017 I/O GATE ARRAY BLOCK DIAGRAM



VDP Pin Description (Table 2)

SIGNAL NAME	PIN NO.	I/O	DESCRIPTION
VGG	1	I	Power Supply: +5.2V +5.2V電源
MP4	2	I/O	CPU-VDP Data Bus CPU-VDPデータバス
MP5	3	I/O	CPU-VDP Data Bus CPU-VDPデータバス
MP6	4	I/O	CPU-VDP Data Bus CPU-VDPデータバス
MP7	5	I/O	CPU-VDP Data Bus (LSB) CPU-VDPデータバス(LSB)
CAS	6	0	Column Address Strobe コラム・アドレス・ストローブ信号
RAS	7	0	Row Address Strobe ロウ・アドレス・ストローブ信号
WR	8	0	Memory Write メモリ・ライト信号
OE	9	0	Memory Output Enable メモリ・アウトプット・イネーブル信号
HIZ	10	0	Not used 使用しない
RWM	11	I	CPU-VDP Write CPU-VDPライト信号
HMP	12	I	Not used, pulled up to +5.2V 使用しない。+5Vにプルアップする。
ODS	13	0	DMA clock Xtal (Memory Access Timing) メモリ・アクセス・タイミング用振動子 接続端子(DMAクロック)
ODE	14	I	VDP Ready VDPレディ信号
READY	15	0	VDP-Memory Address/Data Bus (LSB) VDP-メモリ・アドレス/データ・バス(LSB)
D7	16	I/O	VDP-Memory Address/Data Bus (MSB) VDP-メモリ・アドレス/データ・バス(MSB)
D6	17	I/O	VDP-Memory Address/Data Bus VDP-メモリ・アドレス/データ・バス
D5	18	I/O	VDP-Memory Address/Data Bus VDP-メモリ・アドレス/データ・バス
D4	19	I/O	VDP-Memory Address/Data Bus VDP-メモリ・アドレス/データ・バス
D3	20	I/O	VDP-Memory Address/Data Bus VDP-メモリ・アドレス/データ・バス

## CHANGE INFORMATION

### IMPORTANT

The following modifications are mandatory. If any change has not been on a given unit, it must be implemented.

### FUSE

#### • 100V VERSION ONLY

EFF. SN 700750-UP  
F1: SD-6 630mA (12559409)

### CPU BOARD

#### • Add resistor 100Ω to RGB terminals (Fig. A)

EFF. SN 711650-UP

To avoid accidental shorts of power supply if connected to an unspecified cable.

#### • Add diode, R and C to VSYNC circuit. (Fig. B)

EFF. SN 768700-UP

For positive sync between S-50 and CRT shorten VSYNC pulse width from 1.3ms to 0.3ms.

### CAUTION:

The following S.Numbered products have been retrofitted insufficiently with a 68k resistor, getting 0.5ms pulse. Change the resistor to 47k as required.

SN 711950-712199

SN 712250-712799

SN 712900-768699

#### • Changing the values of CPU A/D input resistors (Fig. C)

R21-24: 10KΩ to 1KΩ

Improve S/N ratio at A/D converter input.

(Aftertouch CV occasionally does not fall down to 0V against 0 setting.)

### CPU BOARD

#### • Add a capacitor to WAVE GATE ARRAY CLOCK GENERATOR (Fig. D)

EFF. SN 711650-UP

For more stable oscillation.

#### • Change S/H capacitor C12 0.01μF to 0.01μF

EFF. SN 711650-UP

To improve S/N ratio.

### JACK BOARD

#### • Change

C55-C58: Mylar 0.001μF to Ceramic 470pF

C54: Mylar 0.0022μF to Ceramic 470pF

C53: Ceramic 100pF to Ceramic 22pF

EFF. SN 700655-UP (100V version)

700750-UP (117V version)

701605-UP (220V version)

701625-UP (240VE version)

701635-UP (240VA version)

To improve S/N ratio.

## 変更案内

### 重要

修理等の場合は製造番号を確認し、下記の変更が実施されているかを調べて下さい。

未実施の場合は、本枠内の変更を必ず行って下さい。

### ■ヒューズ

#### • 100V仕様のみ値変更

実施 製番 700750 以降  
F1: SD-6 630mA (12559409)

### ■CPUボード

#### • RGB端子抵抗100Ω追加 Fig.A

実施 製番 711650 以降  
理由: 指定外ケーブル接続における電源短絡防止

#### • VSYNCのパルス幅改善(抵抗、コンデンサ、ダイオード追加) Fig.B

1.3 ms → 0.3 ms 実施 製番 768700 以降  
注意: 製番 711950-712199  
712250-712799  
712900-768699

の製品には、すでに抵抗、コンデンサ、ダイオードが追加実装済です。しかし、抵抗値が 68KΩ (VSYNC パルス幅 0.5 ms に設定) のため、これを 47KΩ に変更して下さい。

理由: 一部 CRT との同期ズレ防止

#### • CPU A/D 入力部の抵抗値変更 Fig.C

R21-24: 10KΩ → 1KΩ

実施 製番 725750 以降

理由: A/D 変換部の S/N 改善

[アフタータッチの CV が 0V まで下がりきらない場合があり、これが発音及び MIDI 送信データに影響を与える。]

### ■CPUボード

#### • WAVE GATE ARRAY クロック部コンデンサ追加 Fig.D

実施 製番 711650 以降

理由: 発振の安定化

#### • S/H 回路部コンデンサ(C12)定数変更

実施 製番 711650 以降

マイラ 0.001μF → マイラ 0.01μF

理由: S/H の向上

### ■ジャックボード

#### • コンデンサ定数変更

実施 製番 100V 700655 以降

117V 700750 以降

220V 701605 以降

240VE 701625 以降

240VA 701635 以降

C55-C58: マイラ 0.001μF → セラミック 470pF

C54: マイラ 0.0022μF → セラミック 470pF

C53: セラミック 100pF → セラミック 22pF

理由: S/H の向上

#### • Add resistors to headphone jack (Fig. E)

EFF. SN 723750-UP  
To minimize distortion.

#### • Change

EFF. SN 723750-UP

C1, C2, C13, C14, C25  
C26, C33, C34, C63, C69

→ Change to jumper wire

R80, R81

C35, C36, C82, C83 : Ceramic 330pF to 470pF

R57, R58, R67, R68 : 33KΩ to 15KΩ

C27, C28, C37, C38 : Ceramic 100pF to 47pF

R84 : 4.7KΩ to 22KΩ

To improve S/N ratio.

#### • ヘッドホンジャック抵抗 R119:220Ω追加 Fig. E

実施 製番 723750 以降

理由: ヘッドホン出力の歪防止

#### • 抵抗及びコンデンサ定数変更

実施 製番 723750 以降

C1, C2, C13, C14, C25

C26, C33, C34, C63, C69

→ 削除、ジャンパー線挿入

R80, R81

C35, C36, C82, C83 : セラミック 330pF → セラミック 470pF

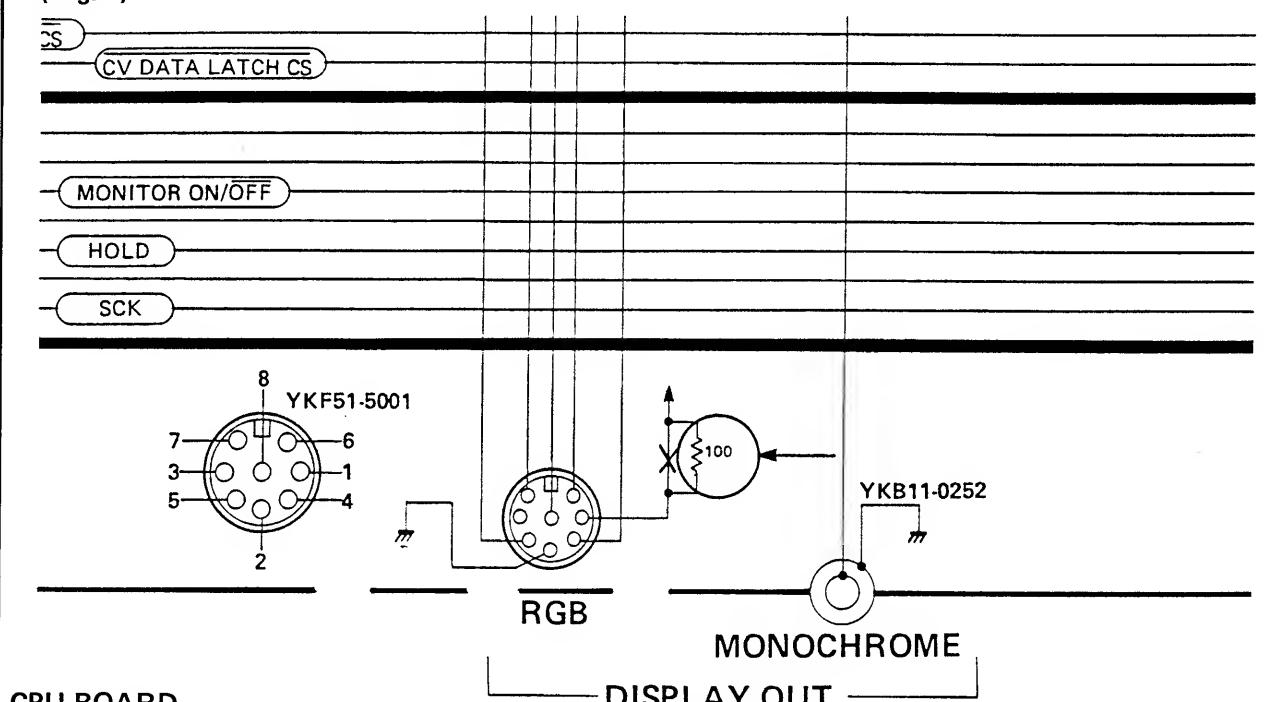
R57, R58, R67, R68 : 33KΩ → 15KΩ

C27, C28, C37, C38 : セラミック 100pF → セラミック 47pF

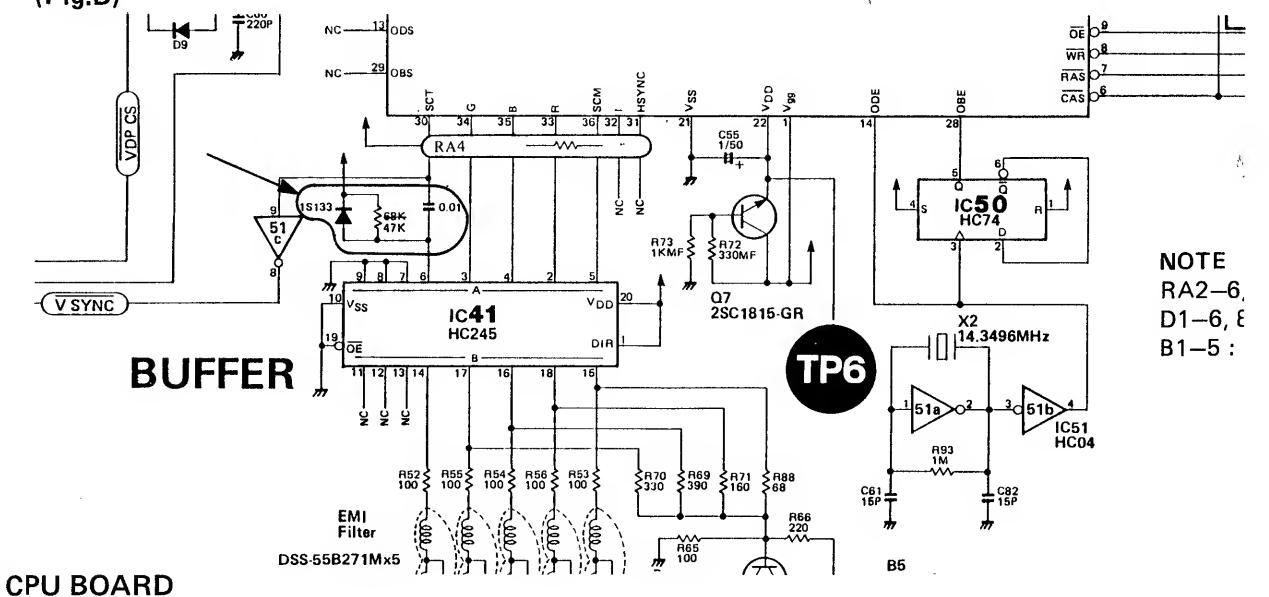
R84 : 4.7KΩ → 22KΩ

理由: S/H の向上

(Fig. A)



(Fig. B)

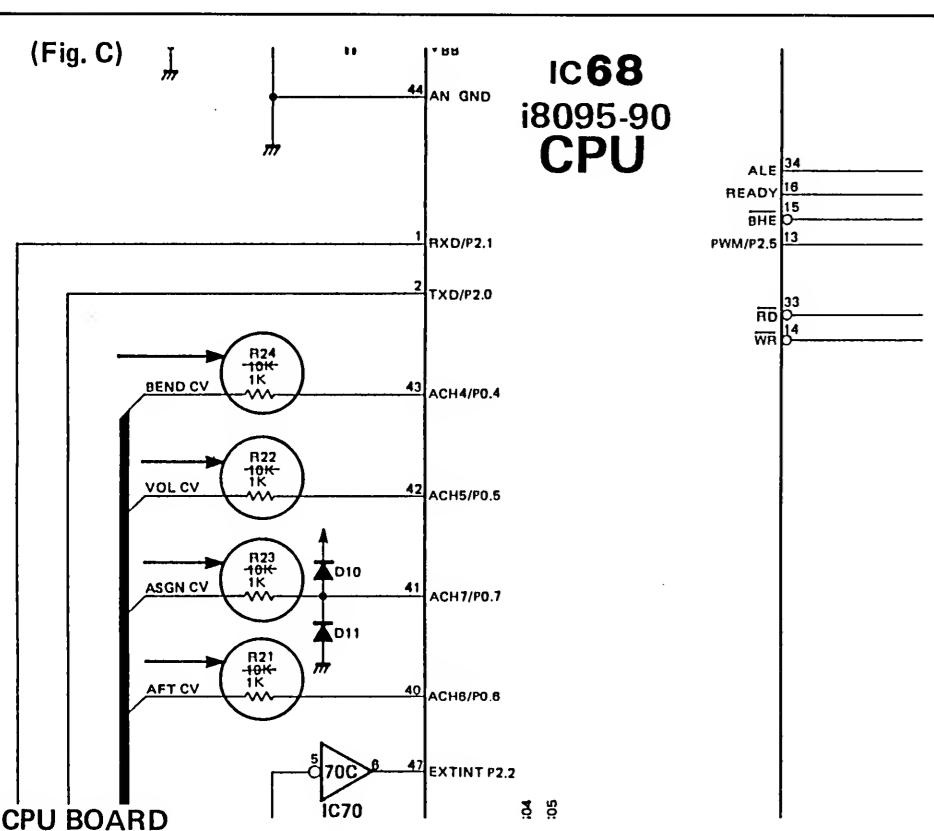


### ROM AND SYSTEM DISC VERSION DISPLAY

This procedure is applicable only to Disk Version 1.0.  
NOTE:  
Label Ver. 1.0 on a system disk represents software versions 1.00 to 1.09. Of these versions, Ver. 1.00 does not contain program for this mode.  
System disk labelled Ver. 2.0 does not run Version Display routine in the way described here. Contact local Roland service facilities for the procedure.

1. Connect the CRT to the unit.
2. Turn the CRT and the unit.
3. Load a system disk labelled Ver. 1.0.
4. Press a FUNC, P1 and SHIFT in that order. (Menu 11 "MASTER" selected.)
5. Press 1 and then ENTER.

The CRT will show the version number of currently installed software in the disk and ROM, respectively (Fig. 1).



### DISK LOAD ERROR MESSAGE NUMBER

Fig. 2 shows the bit definition of FDC internal status register. The bits 2 – 4 are error flags. If an error shown in Table 1 occurs, corresponding flag will be set to "1" level. Error message is represented in hexadecimal number which is converted from the value of status registers (8 bit).

### ADJUSTMENT

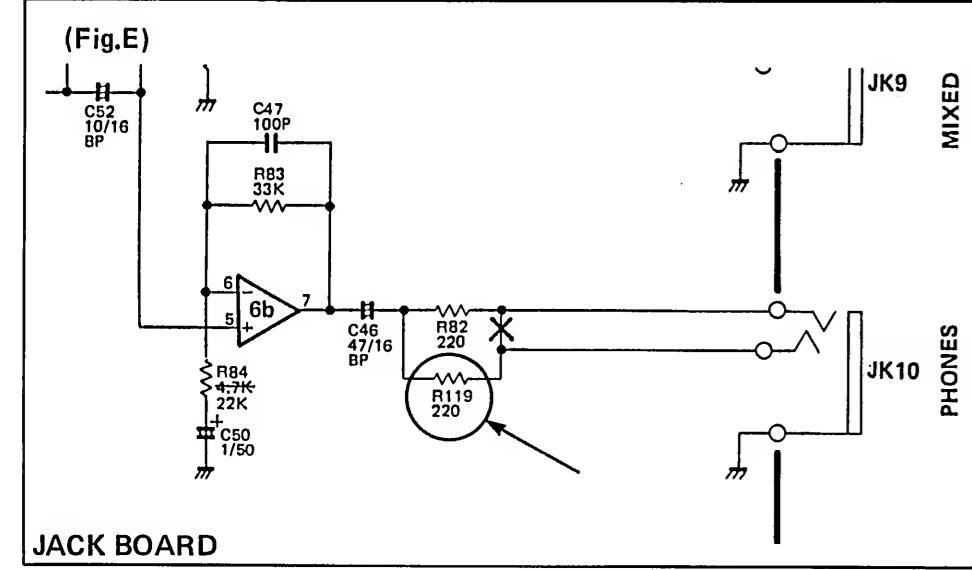
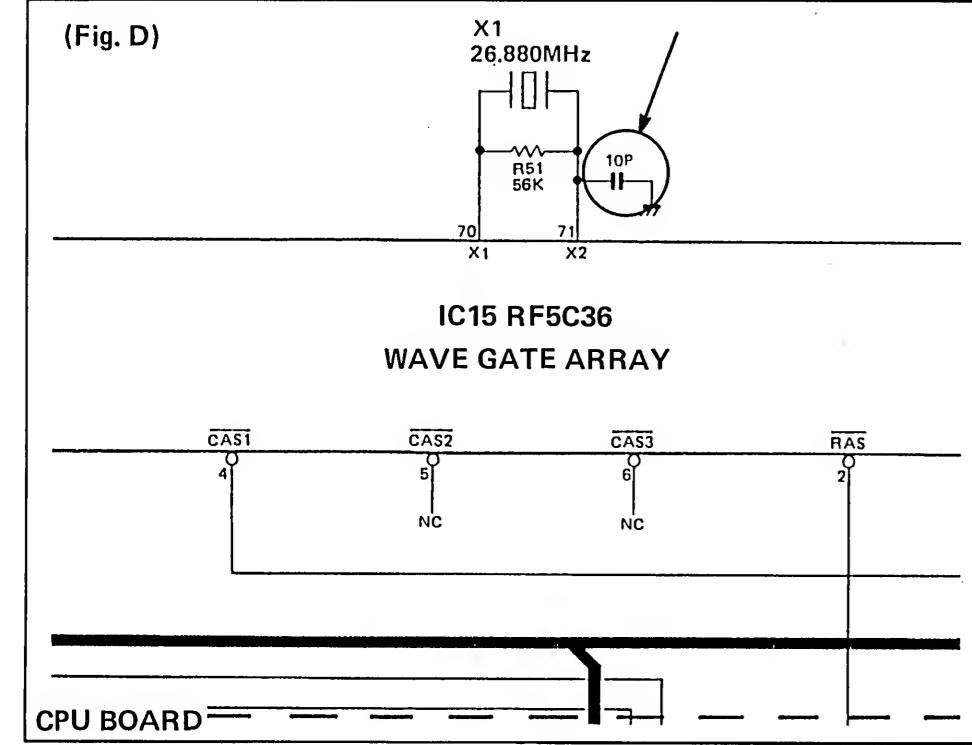
#### ■DC VOLTAGE

- Connect probes of a voltmeter to TP+5 (+5.2V) on the JACK board and TP1 (GND) on the CPU board.
- Adjust VR1 on the power board for +5.2V.

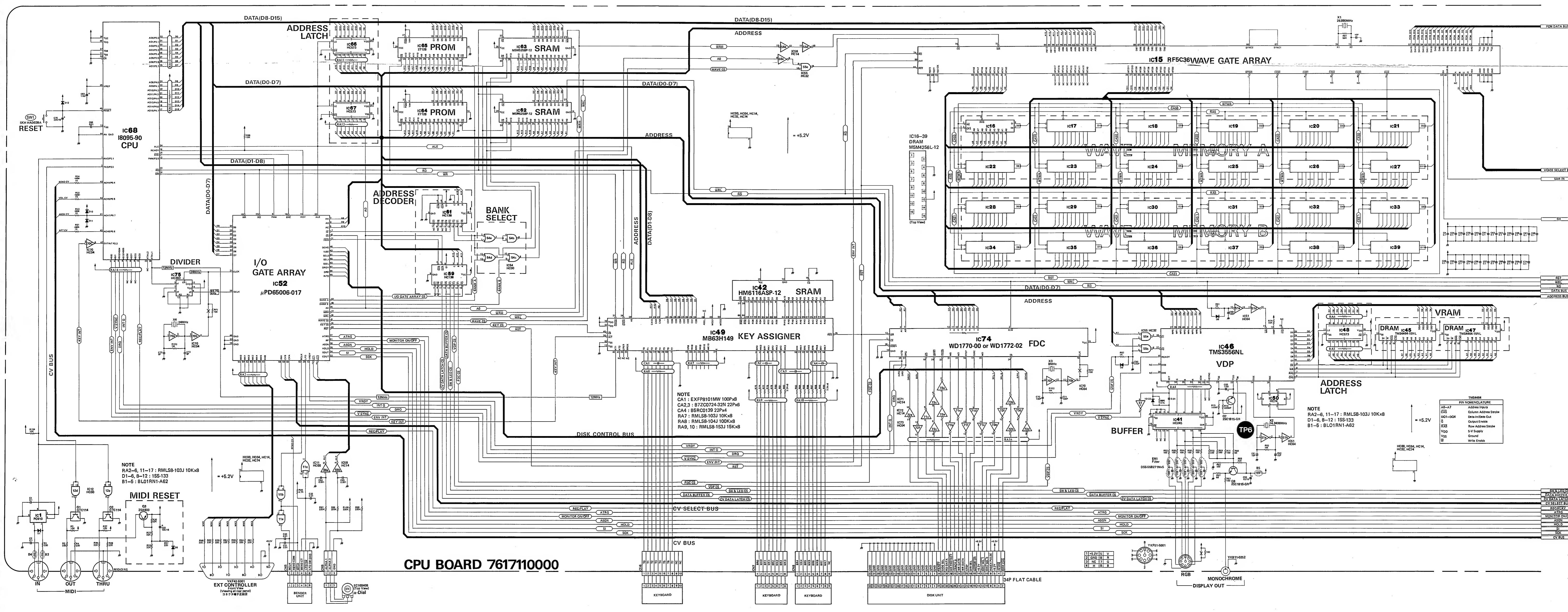
#### ■DC OFFSET

NOTE:  
Softwares implemented in the system disks labelled Ver. 2.0 and above require another procedure to work.

- Turn the unit off.
- Connect an RGB type CRT to RGB socket on the rear panel or a composite type CRT to Composite socket.
- Make sure that no plug is connected to INPUT jack.
- Turn the CRT and unit on.
- Load a system disk.
- After bootstrapping system program, press REC to enter the sampling mode.
- Press P3 and then SHIFT. (Section of menu 13 "WAVE SCOPE".)
- Adjust TRIM1 on the CPU board so that two horizontal lines (signal and reference) overlap.



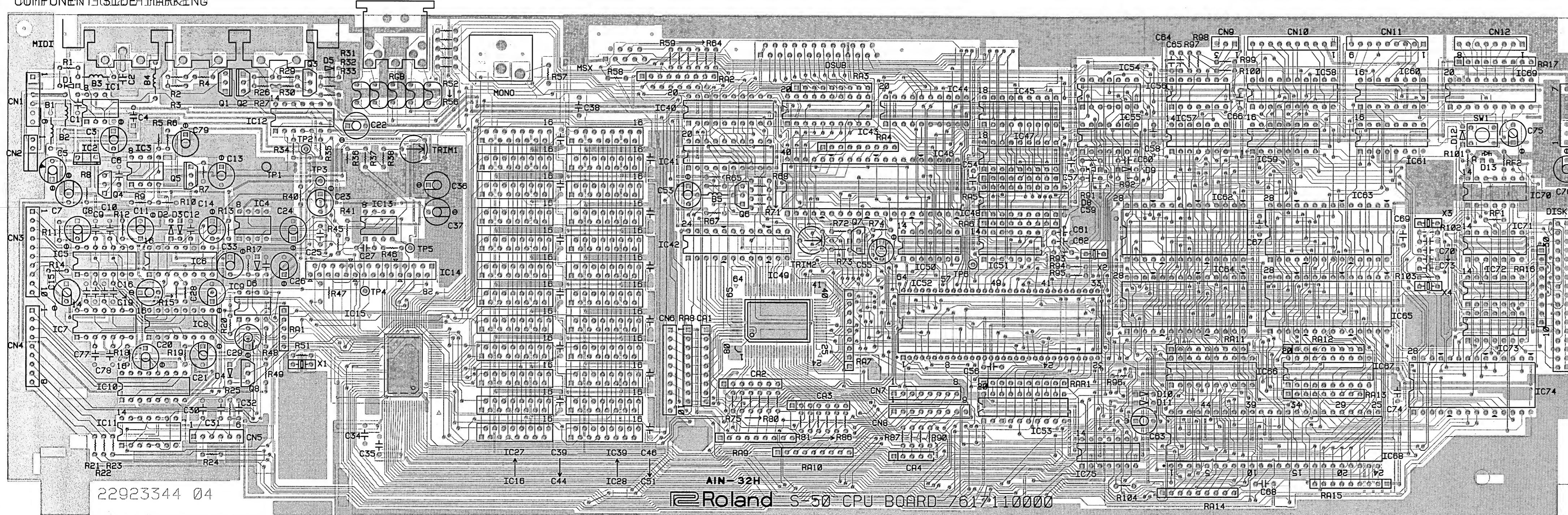
## CIRCUIT DIAGRAM



A  
B  
C  
D  
E  
F  
G  
H  
I  
J  
K  
L  
M  
N  
O  
P  
Q  
R  
S  
T  
U

**CPU BOARD**  
76171100 00  
(pcb 22923344 04)

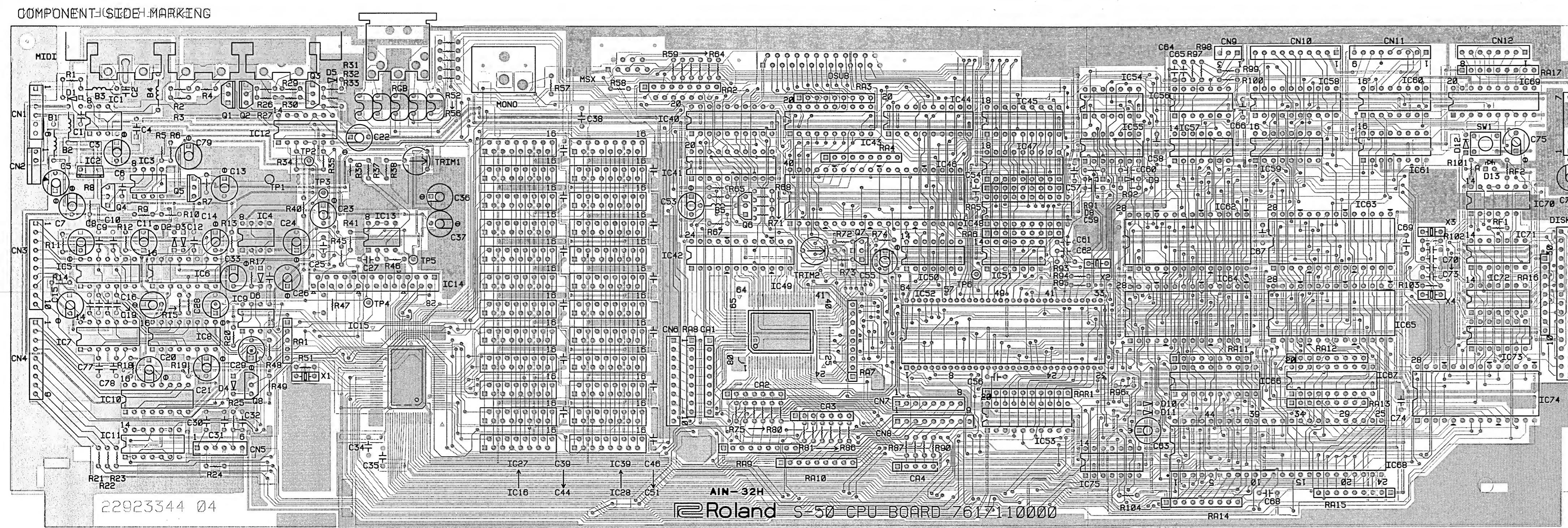
COMPONENT SIDE MARKING



View from component side

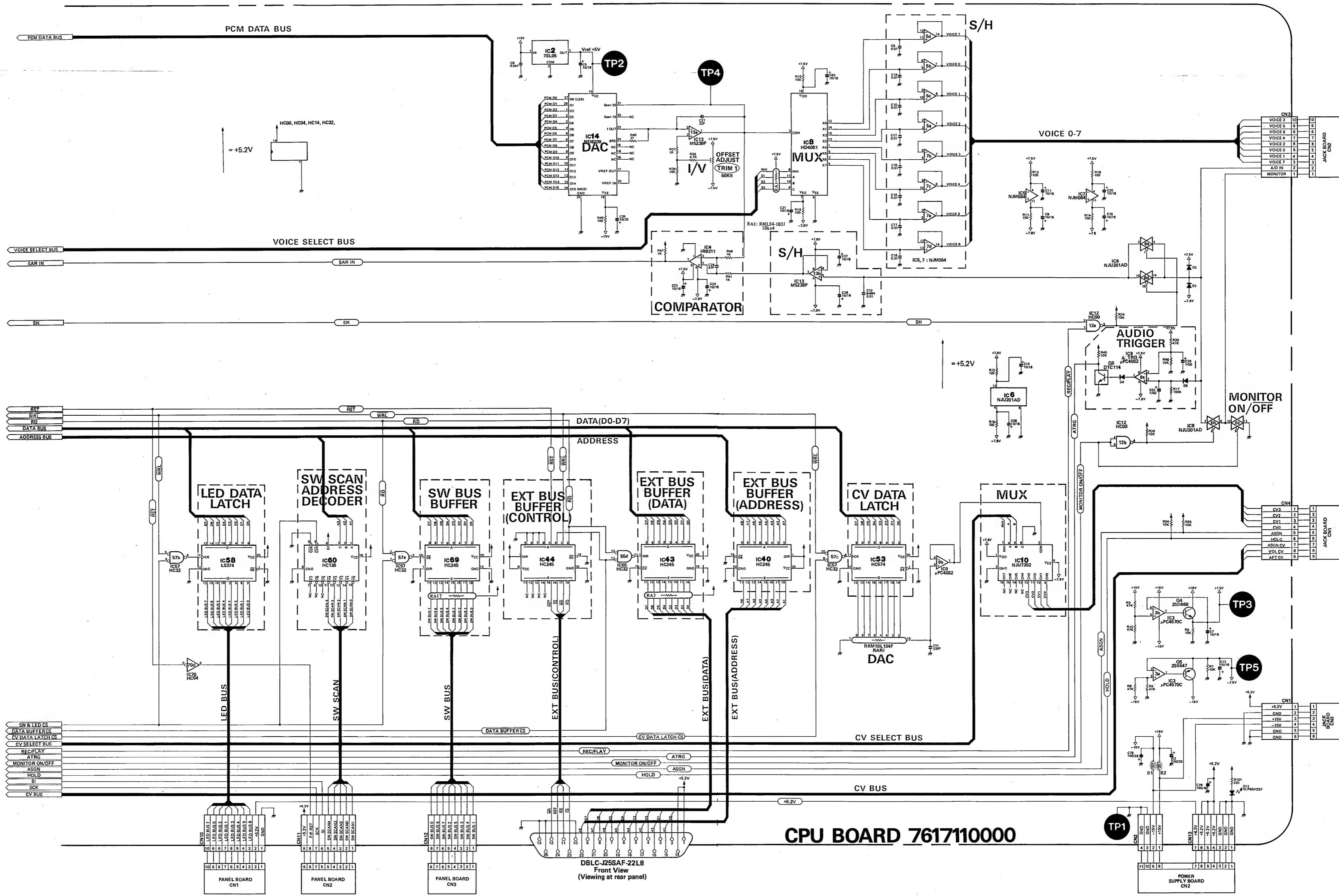
A  
B  
C  
D  
E  
F  
G  
H  
I  
J  
K  
L  
M  
N  
O  
P  
Q  
R  
S  
T**CPU BOARD**  
**76171100 00**  
(pcb 22923344 04)

COMPONENT SIDE MARKING



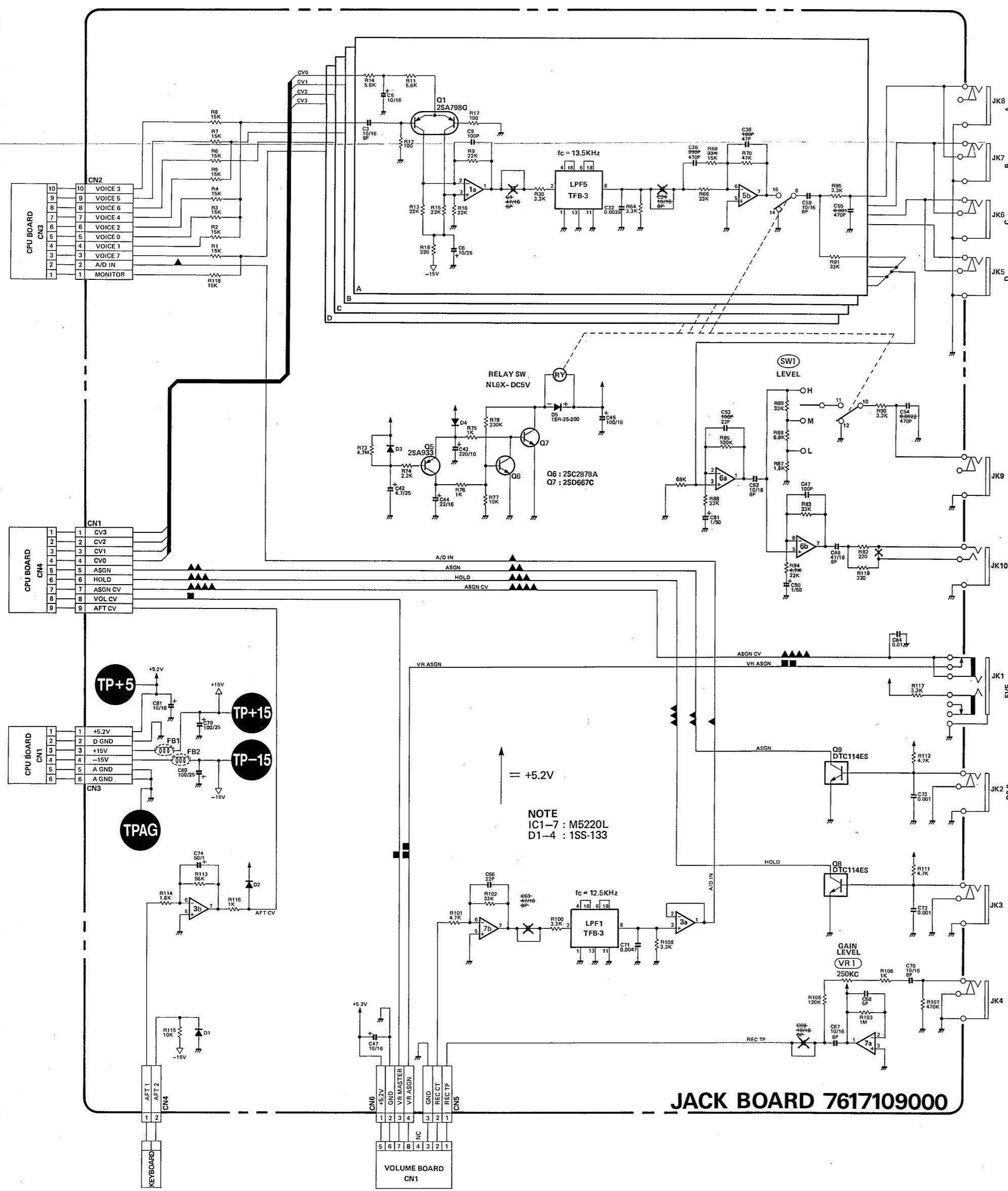
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47

## CIRCUIT DIAGRAM

A  
B  
C  
D  
E  
F  
G  
H  
I  
J  
K  
L  
M  
N  
O  
P  
Q  
R  
S  
T  
U  
V  
W  
X  
Y  
Z

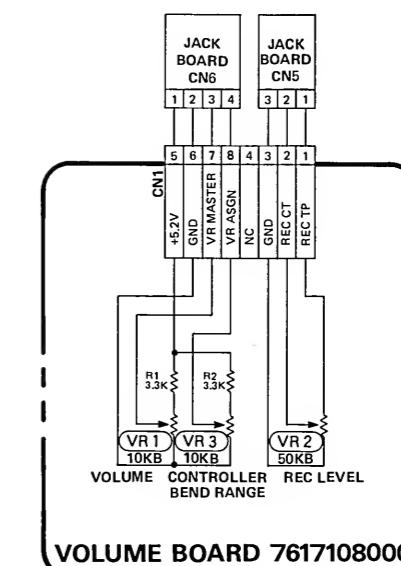
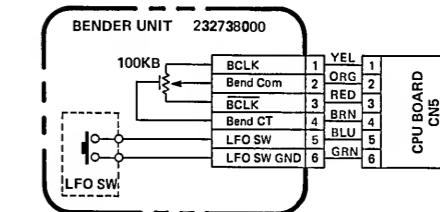
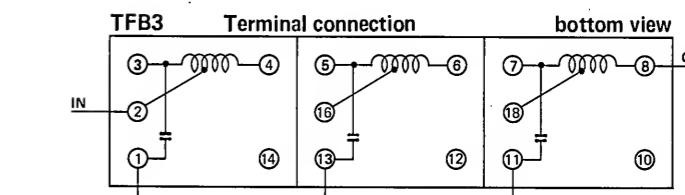
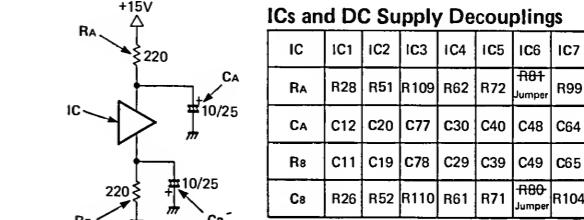
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45

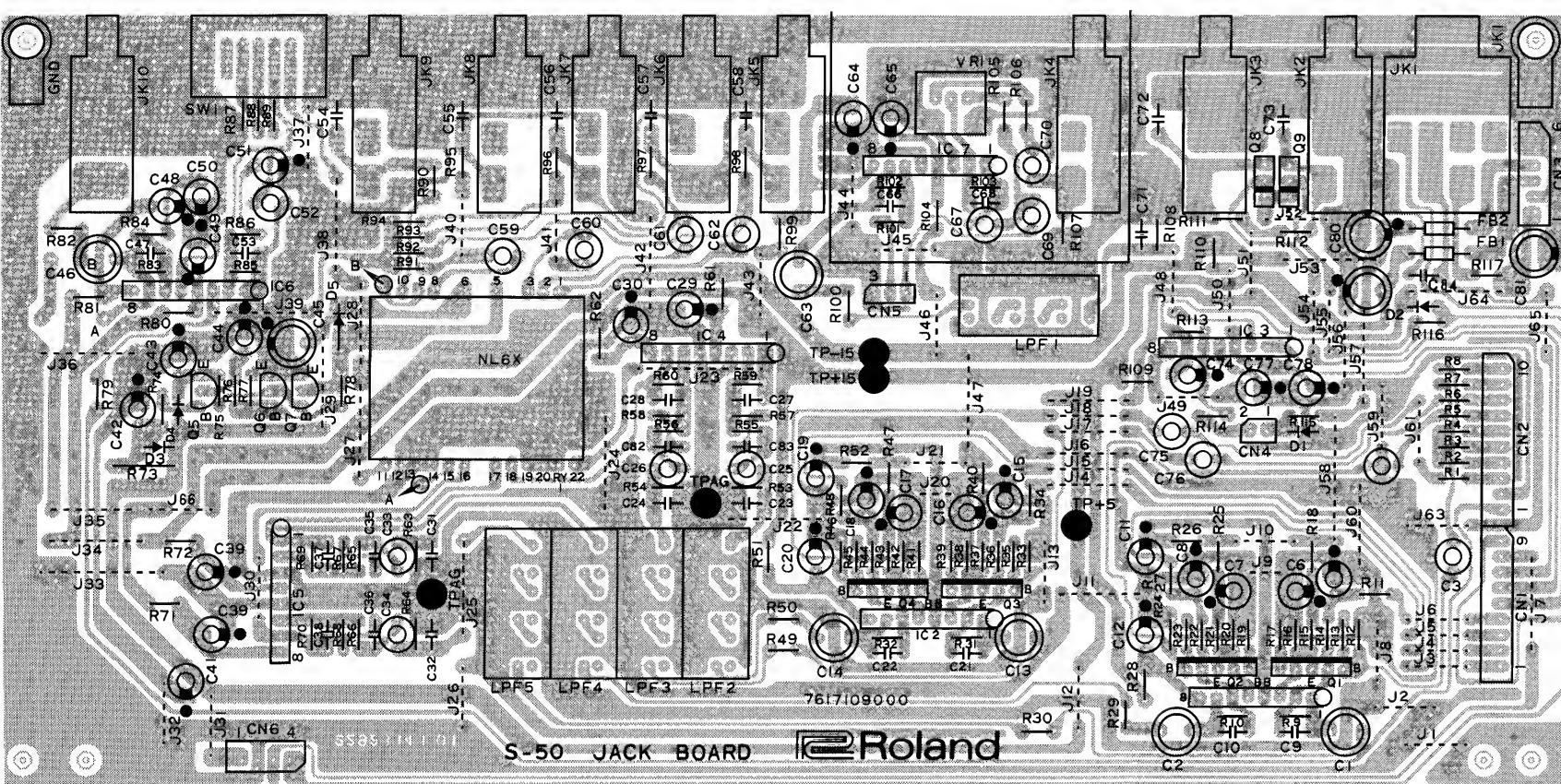
## CIRCUIT DIAGRAM

A  
B  
C  
D  
E  
F  
G  
H  
I  
J  
K  
L  
M  
N  
O  
P  
Q  
R  
S  
T  
U  
V  
W  
X  
Y  
ZCROSS REFERENCE – CIRCUIT NUMBER TO MODULE NUMBER  
(No value difference among modules)

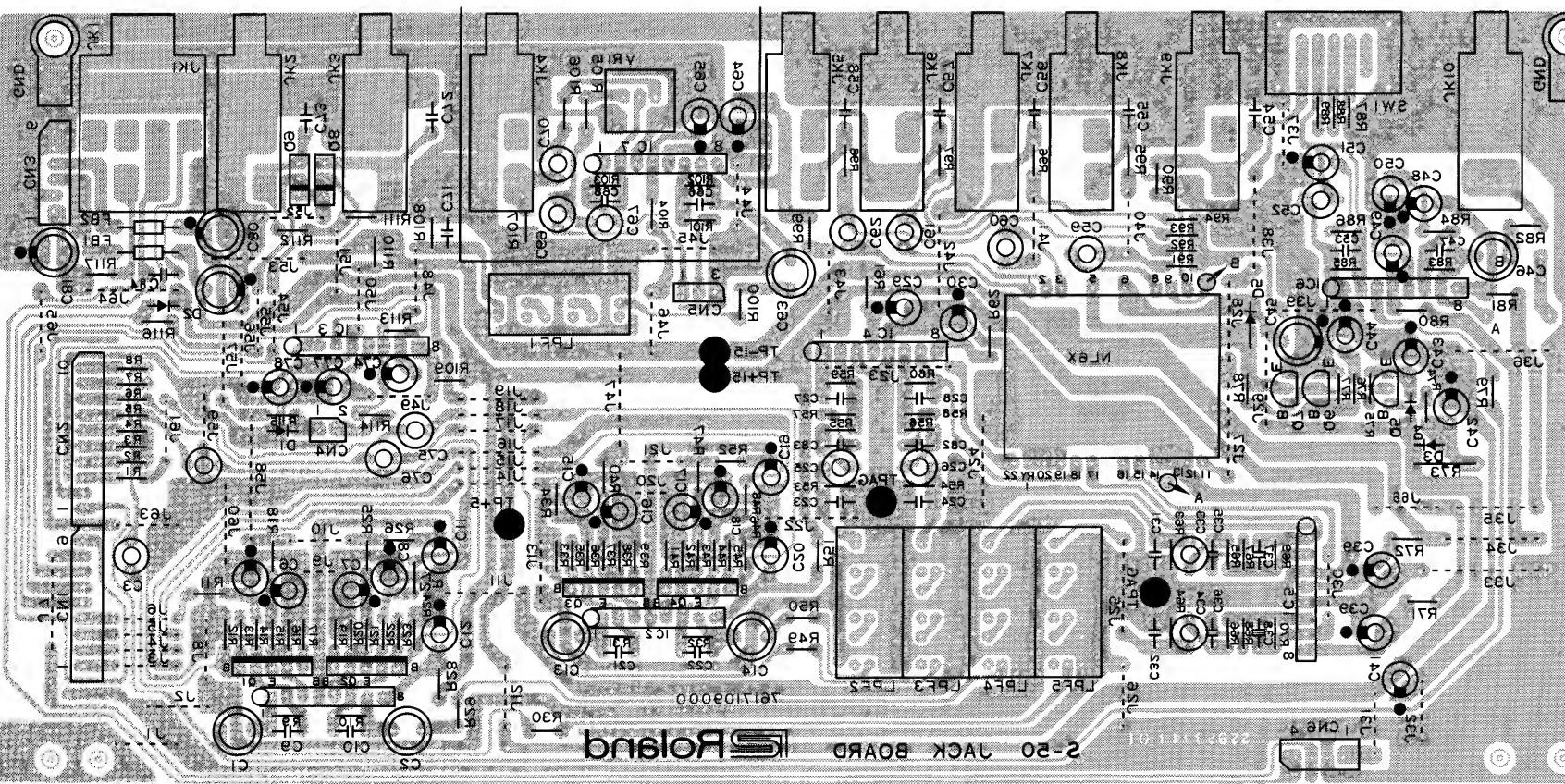
A	C3	R12	Q1	R17	R11	R14	C5	R13	R15	R18	C6	R16	I1a	R9	C9	R30
B	C4	R24	Q2	R19	R22	R27	C8	R23	R21	R25	C7	R20	I1b	R10	C10	R29
C	C76	R33	Q3	R39	R36	R34	C15	R35	R37	R40	C16	R38	I2a	R31	C21	R49
D	C75	R46	Q4	R41	R44	R48	C18	R45	R43	R47	C17	R42	I2b	R32	C22	R50

A	LPF5	C32	R64	C64	R66	C36	R68	I5b	R70	C38	C59	R95	C55	R91
B	LPF4	C31	R63	C63	R65	C35	R67	I5a	R69	C37	C60	R96	C56	R94
C	LPF3	C24	R54	C56	R58	C82	R58	I4b	R60	C28	C61	R97	C57	R93
D	LPF2	C23	R53	C55	R55	C83	R57	I4a	R59	C27	RELAY SW	R58	C58	R92





### View from component side

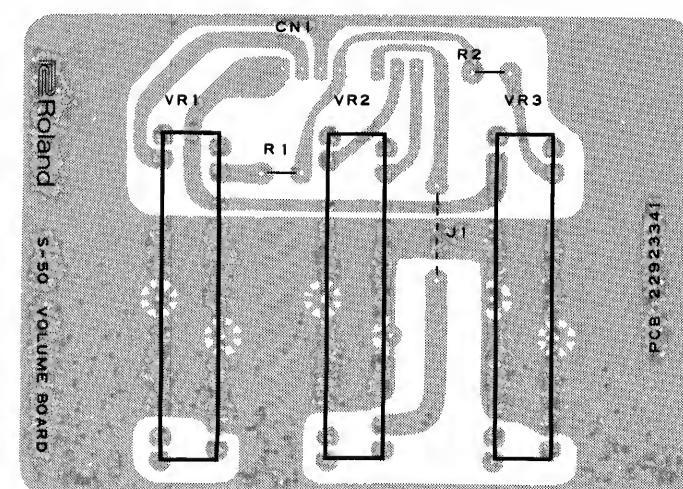


**View from foil side**

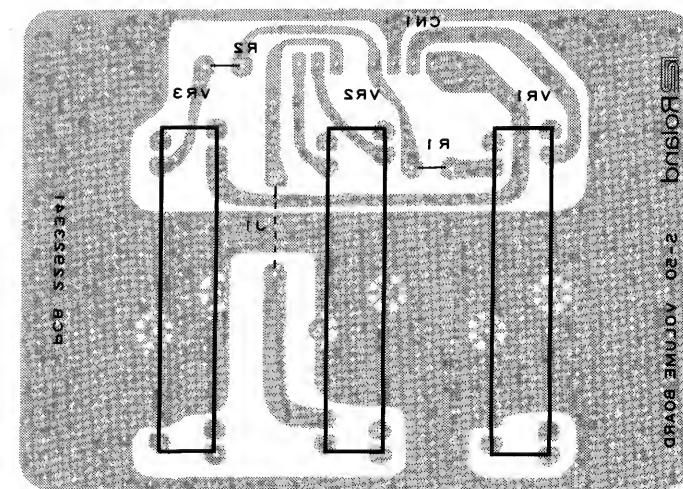
## JACK BOARD

76171090 00

(pcb 22923343 01)

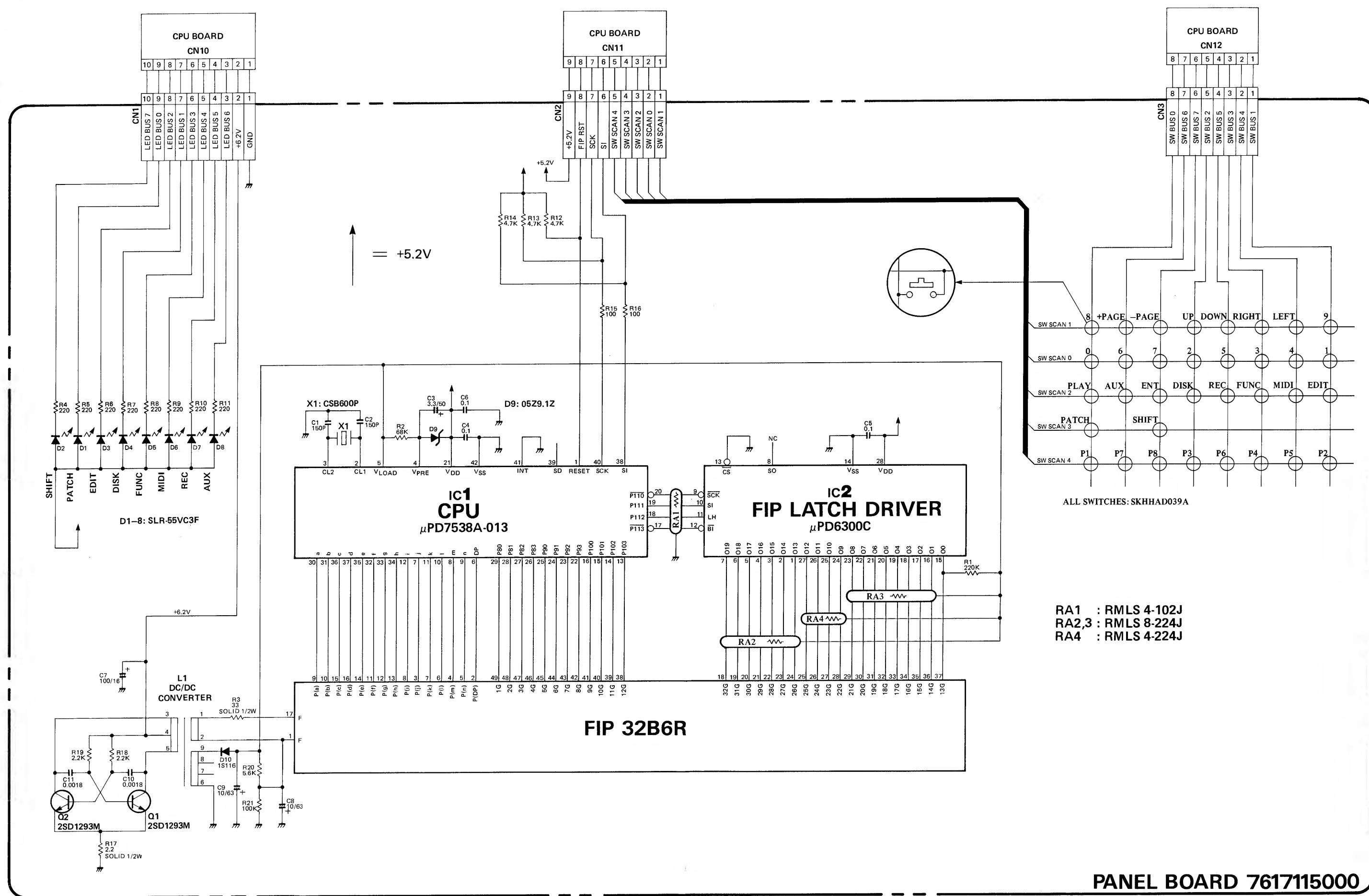


### **View from component side**



### **View from foil side**

## CIRCUIT DIAGRAM



1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39

## A PANEL BOARD

76171150 00

(pcb 22923342 00)

6

6

6

6

6

11

10

1

14

3

1000 1000

IV

14

6

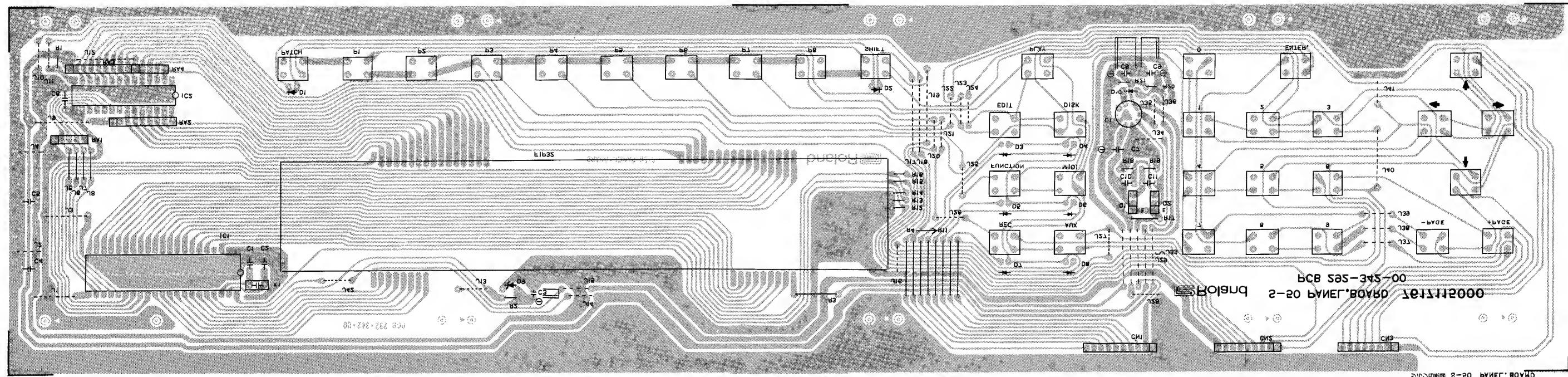
4

Q

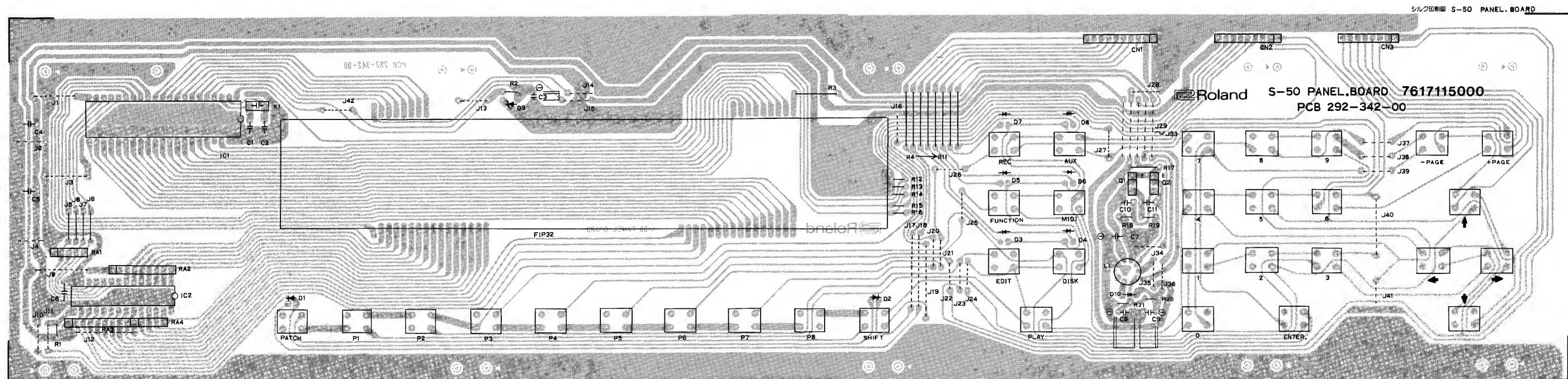
R

5

T

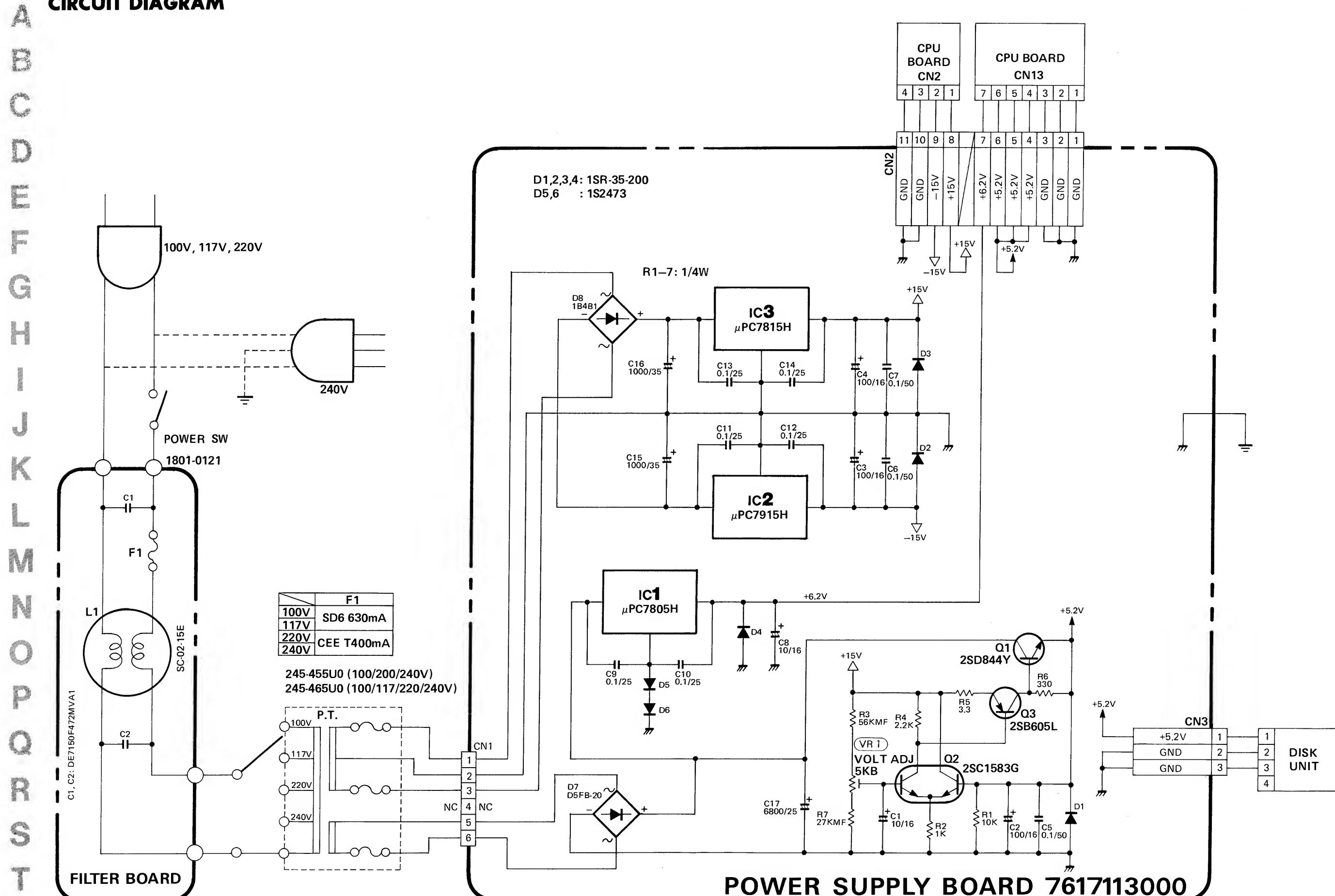


### **View from foil side**



### **View from component side**

## CIRCUIT DIAGRAM



7617112100 100V  
7617112200 117V  
7617112400 220V  
7617112500 240VE  
7617112600 240VA

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38

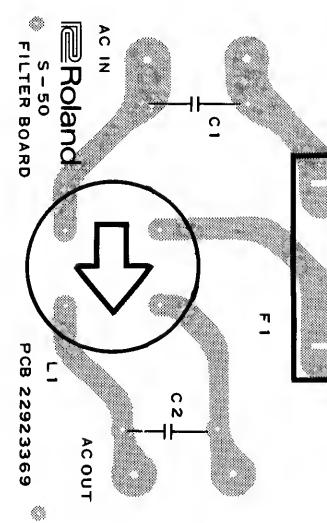
A  
B  
C  
D  
E  
F  
G  
H  
I  
J  
K  
L  
M  
N  
O  
P  
Q  
R  
S  
T**FILTER BOARD**

76171122 00 100/117V

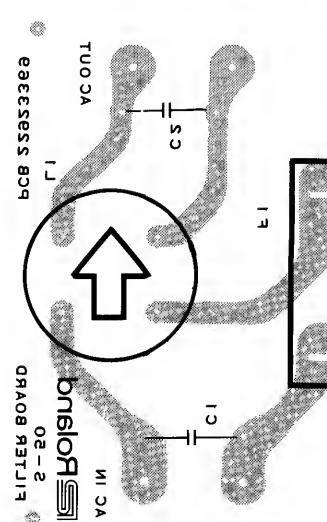
76171124 00 220V

76171125 00 240V

(pcb 22923369 00)



View from component side

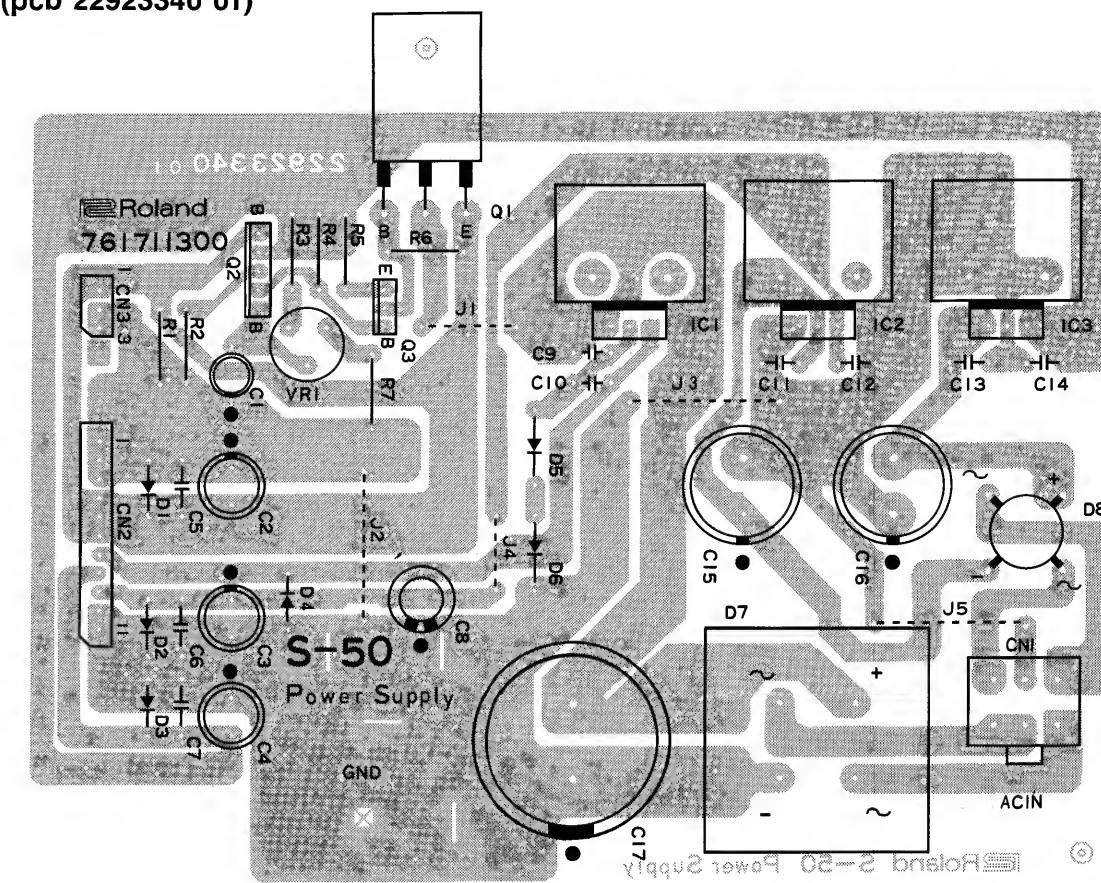


View from foil side

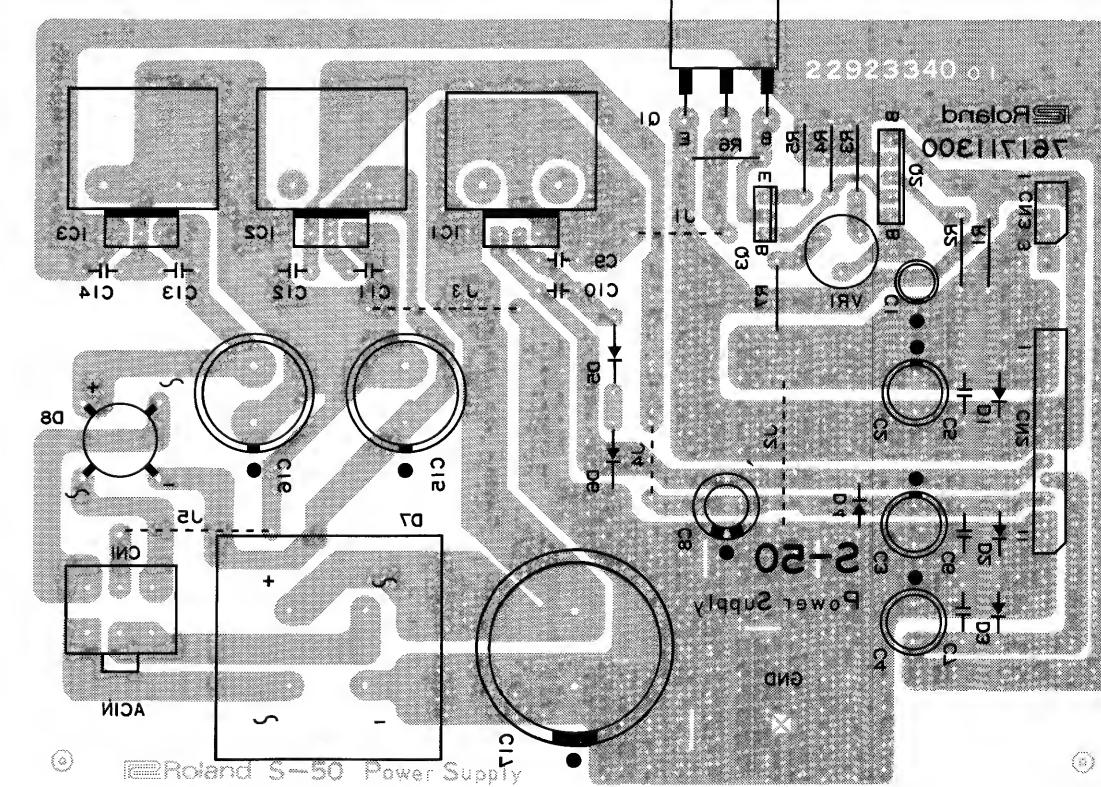
**POWER SUPPLY BOARD**

76171130 00

(pcb 22923340 01)



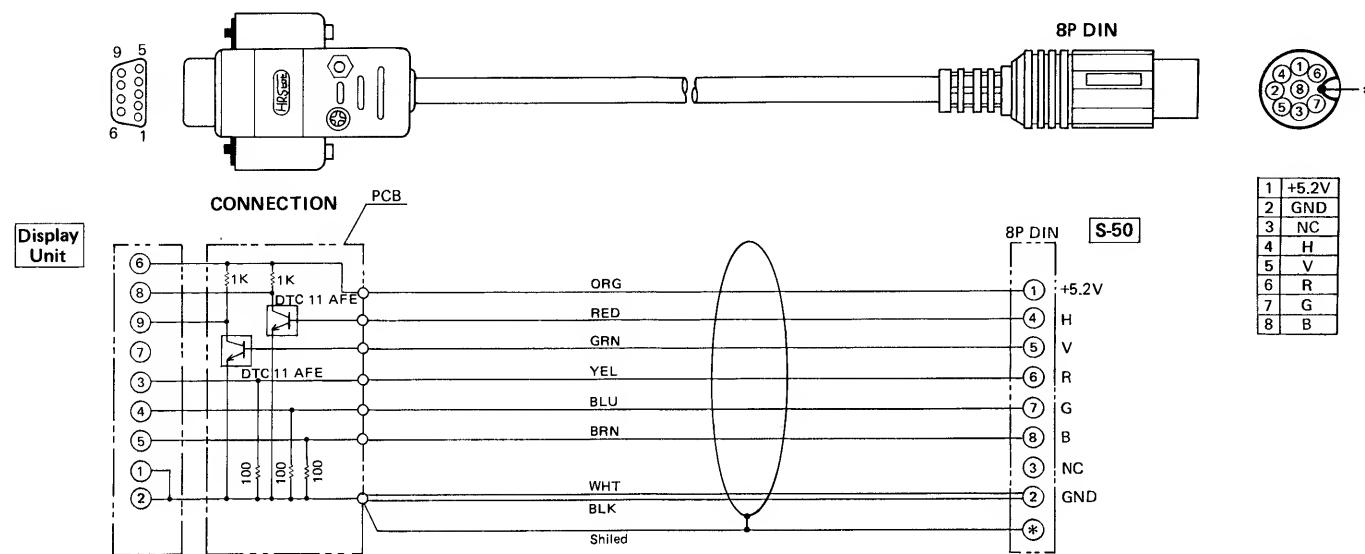
View from component side



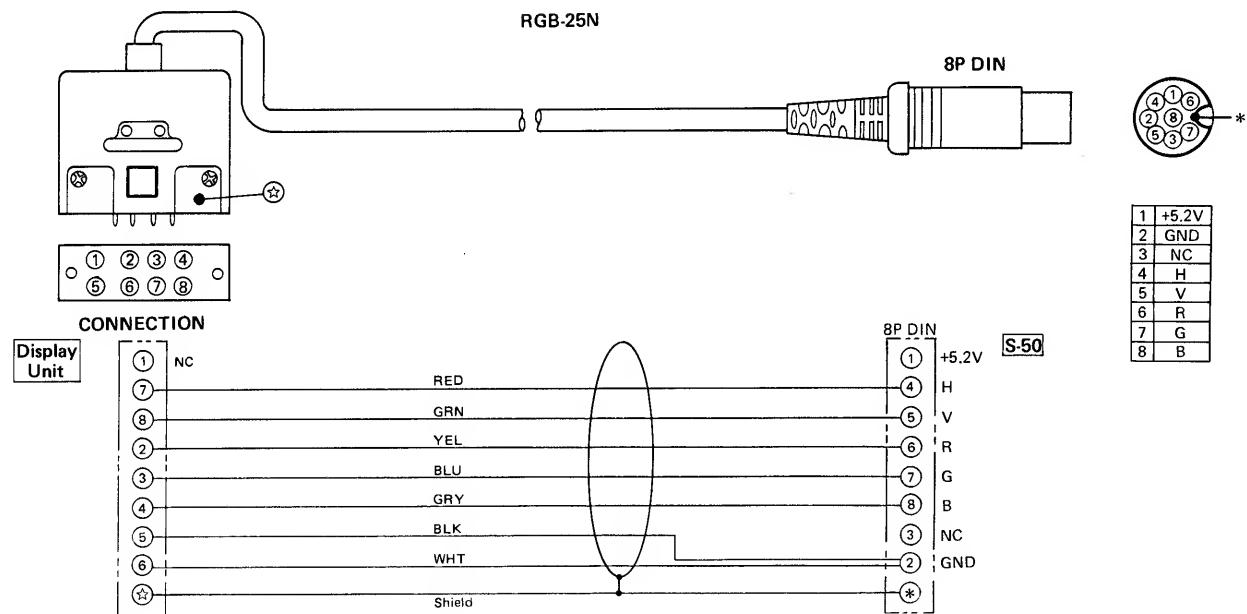
View from foil side

## RGB CABLE

RGB-25I



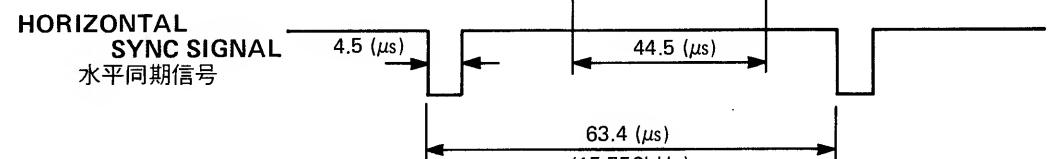
RGB-25N



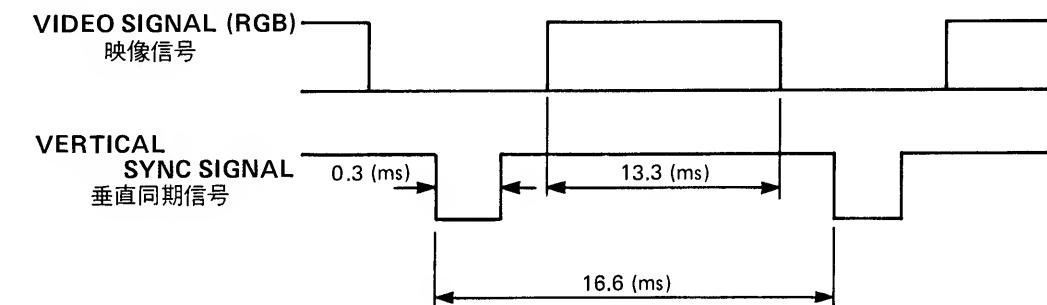
## RGB OUT TIMING CHART

## RGB出力タイミングチャート

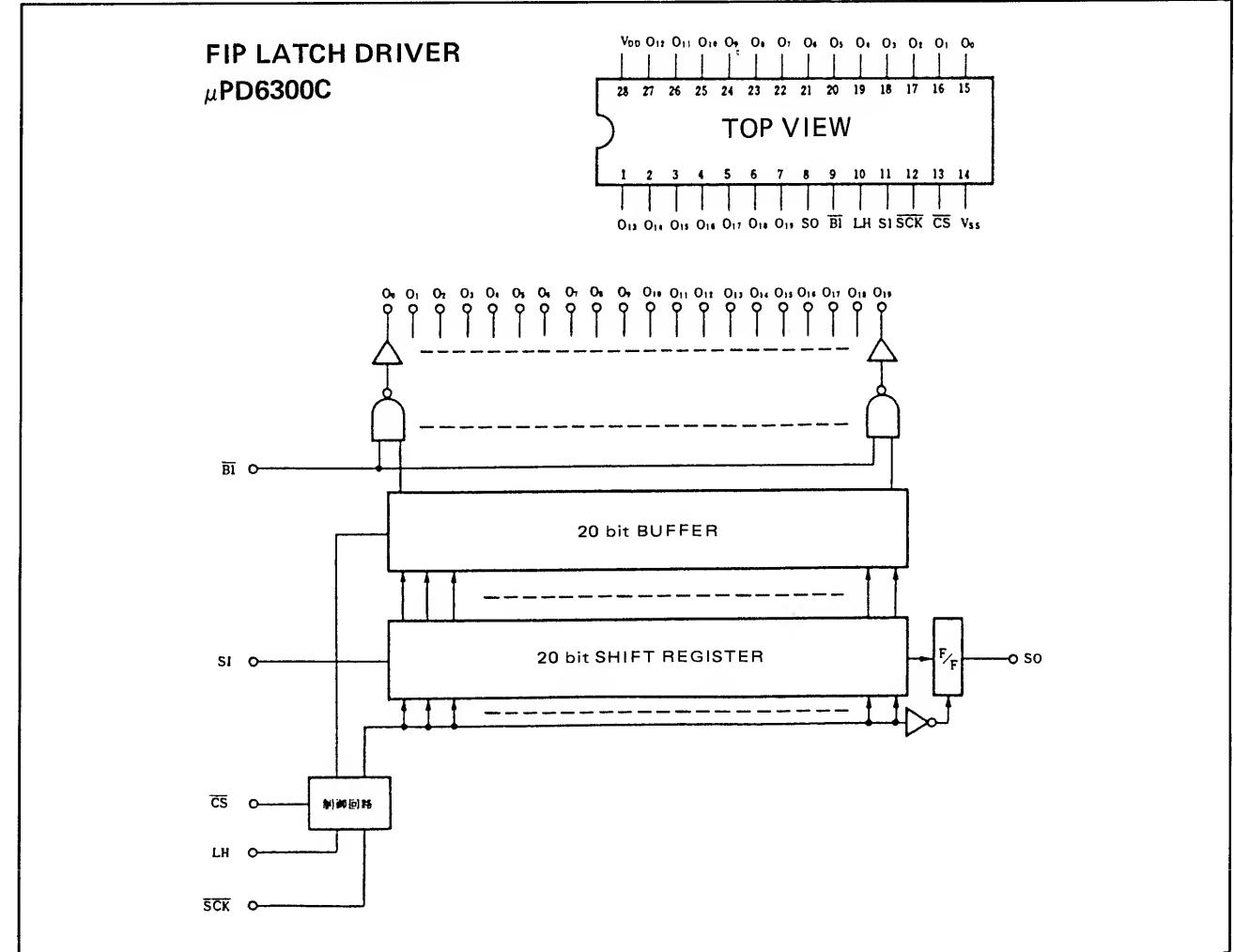
- HORIZONTAL SYNC 水平同期

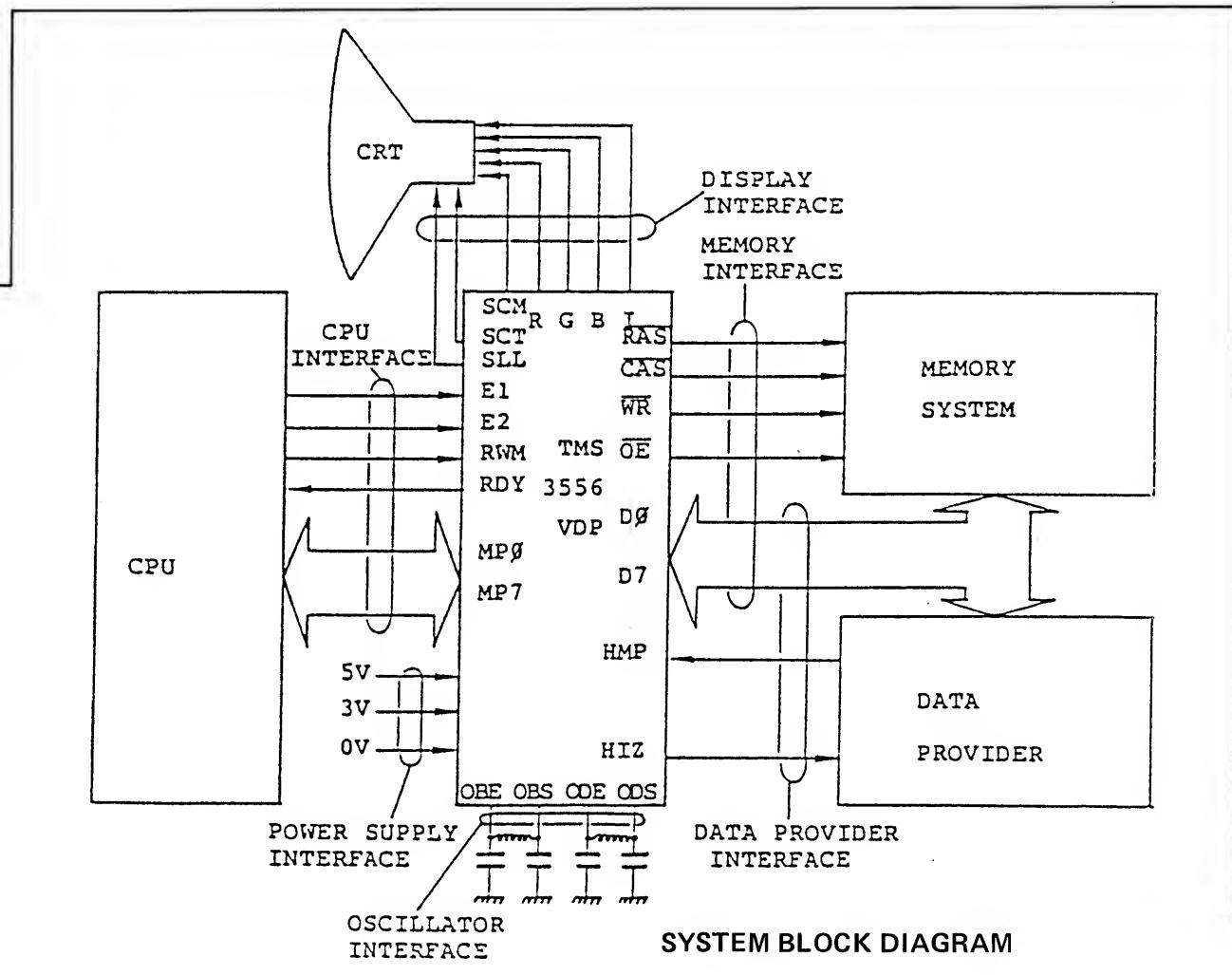
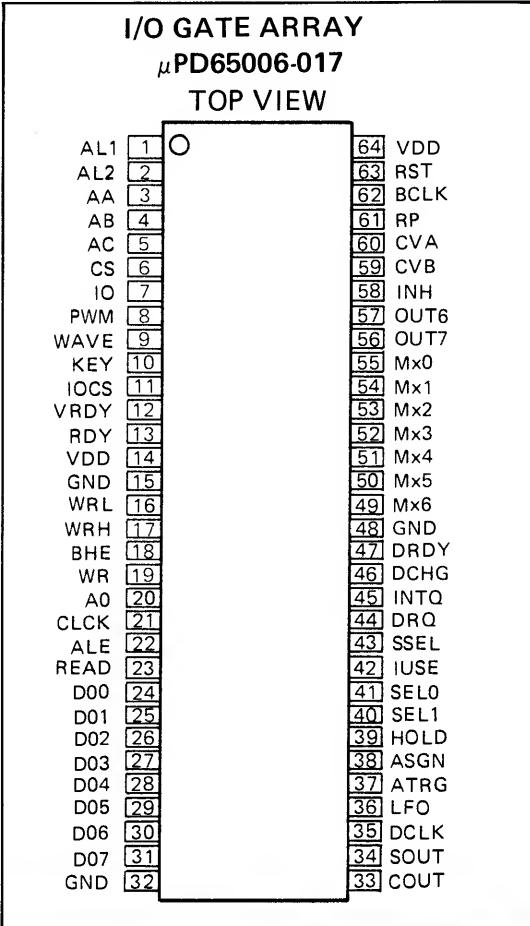
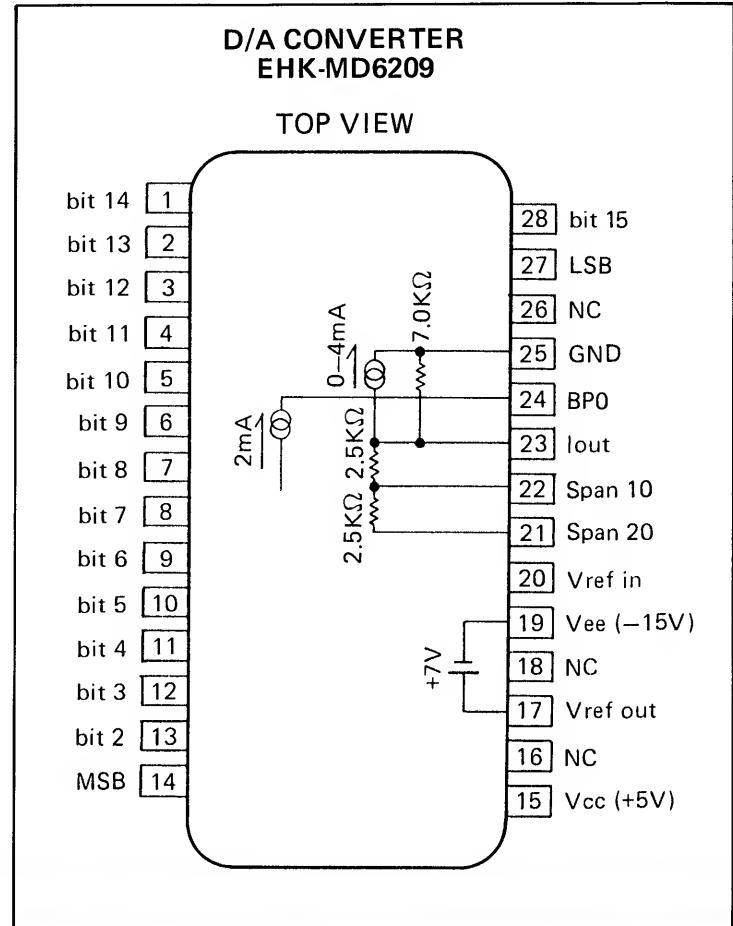
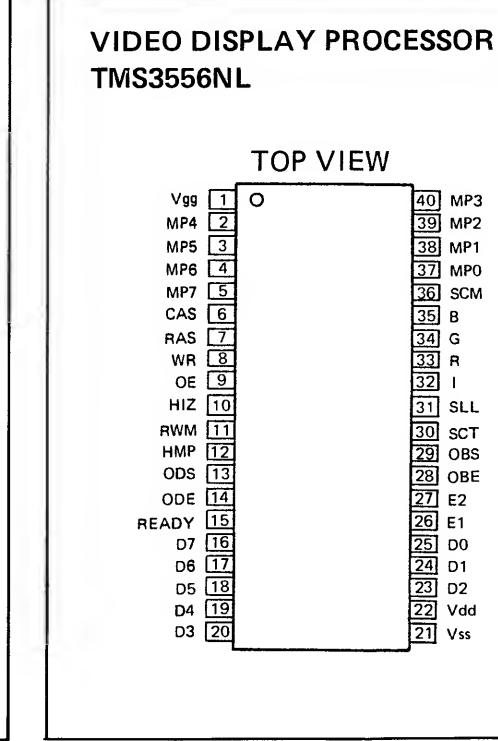
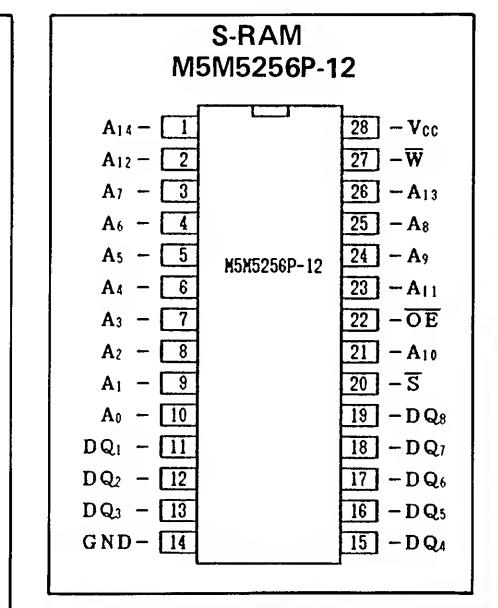
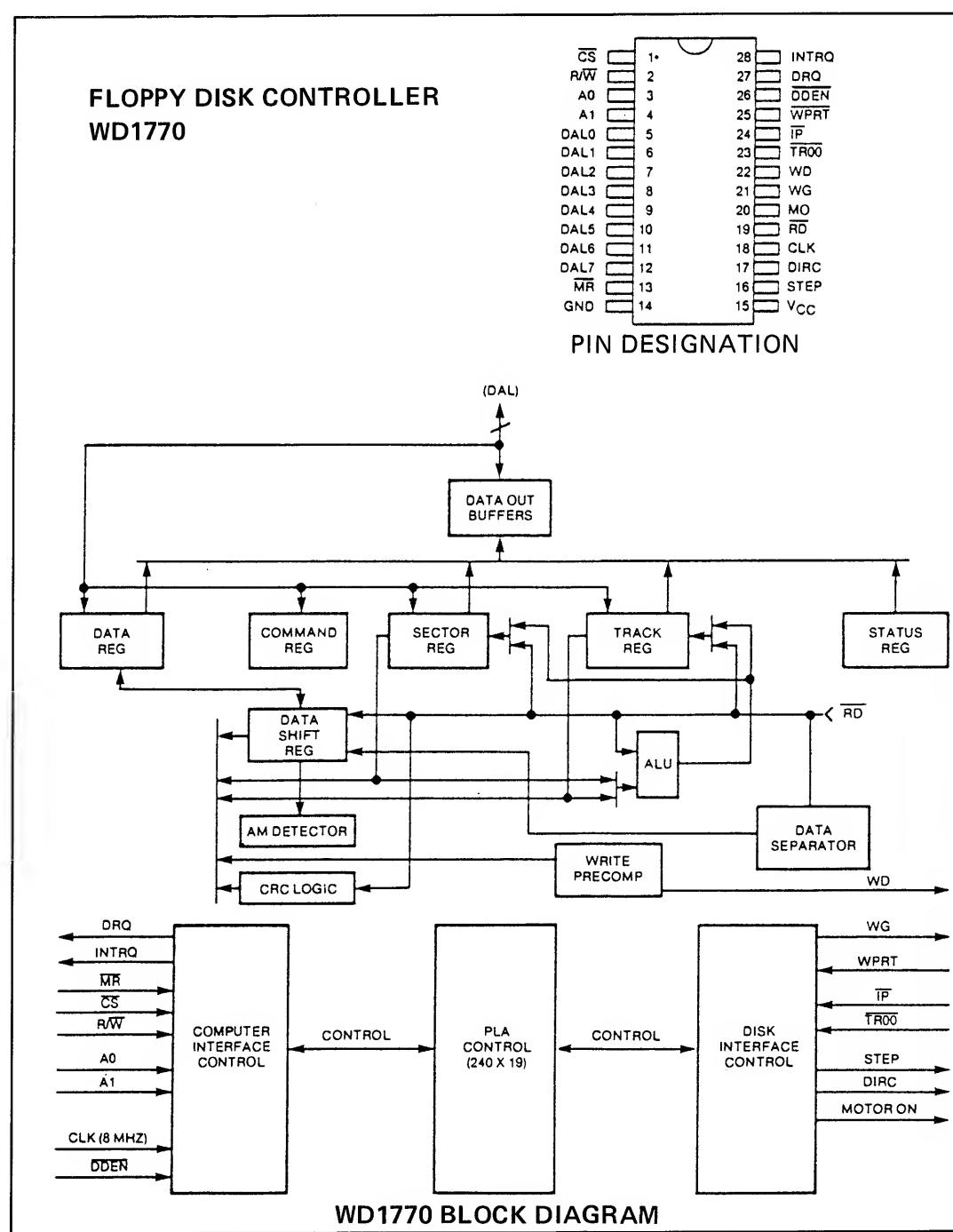
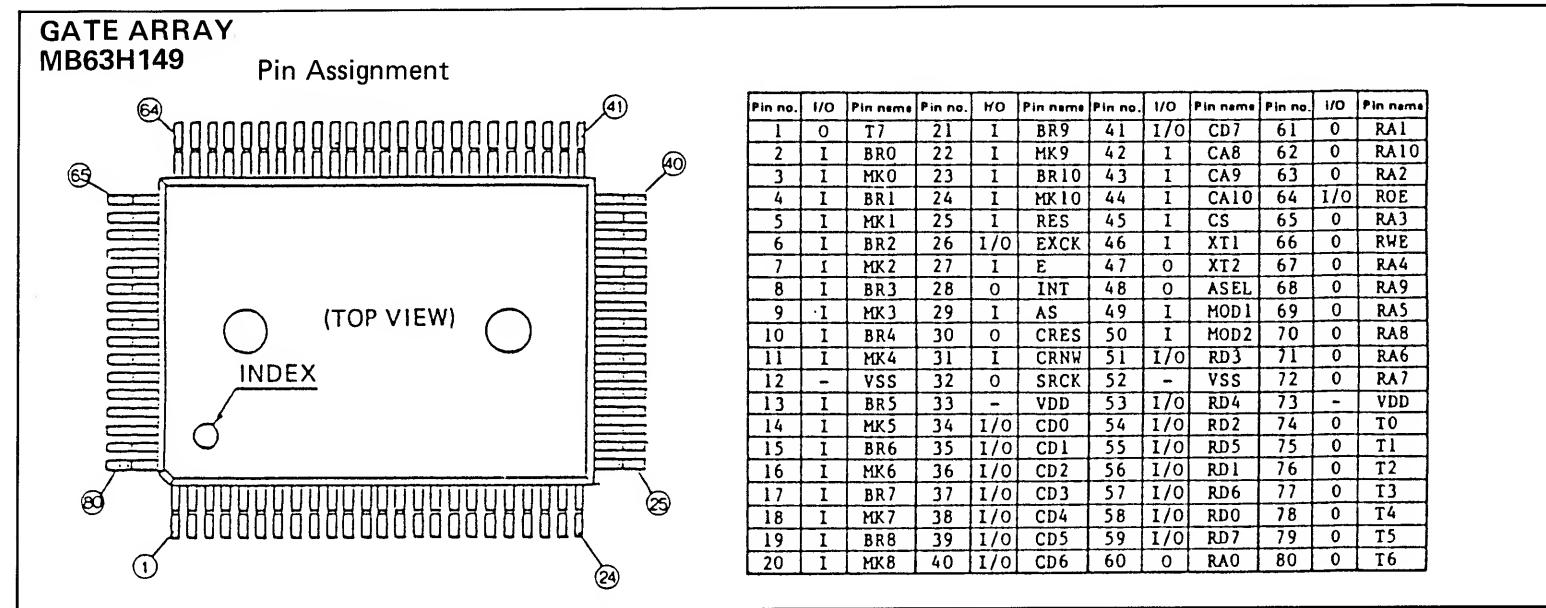


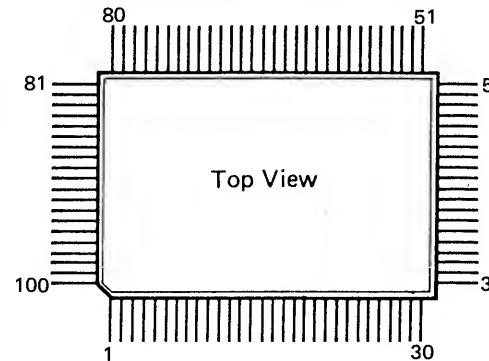
- VERTICAL SYNC 垂直同期



## IC DATA

FIP LATCH DRIVER  
μPD6300C

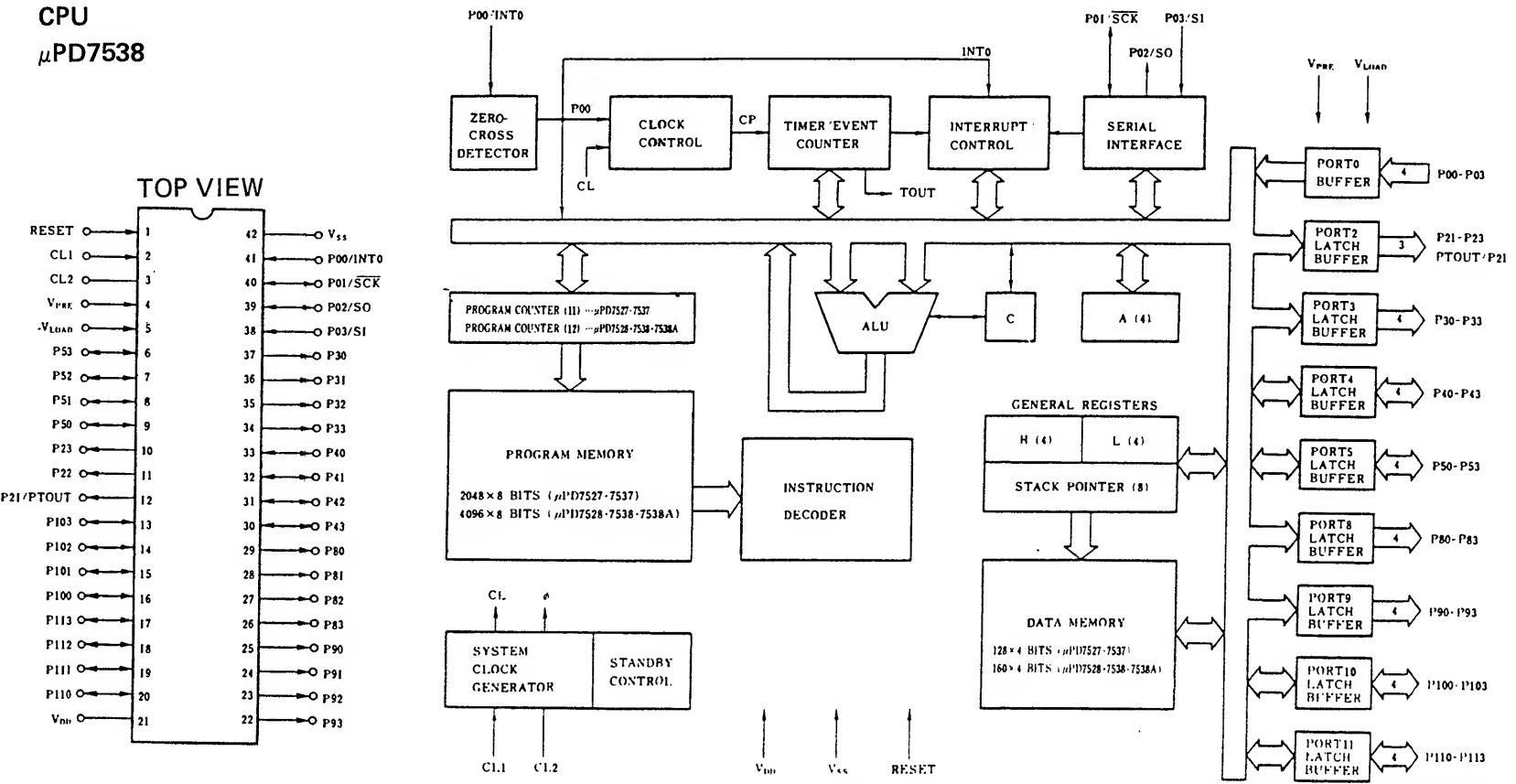


**GATE ARRAY**  
**RF5C36**


PIN No	PIN NAME	I/O	PIN No	PIN NAME	I/O
1	WTWR	0	51	DA9	0
2	RAS	0	52	DA10	0
3	CAS0	0	53	DA11	0
4	CAS1	0	54	DA12	0
5	CAS2	0	55	DA13	0
6	CAS3	-	56	DA14	0
7	VCC	0	57	DA15	0
8	WTAO	0	58	VCC	-
9	WTAI1	0	59	SH	0
10	WTAI2	0	60	MXA	0
11	WTAI3	0	61	MXB	0
12	WTAI4	0	62	MXC	0
13	WTAI5	0	63	MXD	0
14	WTAI6	0	64	INH	0
15	WTAI7	0	65	RST	I
16	WTAI8	0 (NC)	66	SYNO	0
17	WTAI9	0 (NC)	67	SYNI	I
18	WTAI10	0 (NC)	68	TEST2	I
19	WTAI11	0 (NC)	69	TEST1	I
20	WTAI12	0 (NC)	70	XTAL1	XIN
21	WTAI13	0 (NC)	71	XTAL2	XOUT
22	WTAI14	0 (NC)	72	TESTCK	I
23	WTAI15	0 (NC)	73	WR	I
24	WTAI16	0 (NC)	74	RD	I
25	WTAI17	0	75	CS	I
26	GND	-	76	A0	I
27	WTDO	I/O	77	A1	I
28	WTDI	I/O	78	A2	I
29	WTD2	I/O	79	A3	I
30	WTD3	I/O	80	GND	-
31	WTD4	I/O	81	VCC	-
32	WTD5	I/O	82	A4	I
33	WTD6	I/O	83	A5	I
34	WTD7	I/O	84	A6	I
35	WTD8	I/O	85	A7	I
36	WTD9	I/O	86	A8	I
37	WTD10	I/O	87	A9	I
38	WTD11	I/O	88	A10	I
39	VCC	-	89	A11	I
40	SARin	I	90	A12	I
41	GND	-	91	DB0	I/O
42	DA0	0	92	DB1	I/O
43	DA1	0	93	DB2	I/O
44	DA2	0	94	DB3	I/O
45	DA3	0	95	DB4	I/O
46	DA4	0	96	DB5	I/O
47	DA5	0	97	DB6	I/O
48	DA6	0	98	DB7	I/O
49	DA7	0	99	INT	0
50	DA8	0	100	GND	-

\* XIN,XOUT : crystal

\* OUTPUT LOAD CONDITION : CL=100pF

**CPU**  
**μPD7538**


## MIDI IMPLEMENTATION

S-50 M101 IMPLEMENTATION

Version 1.00 Aug. 25 1986

\*\*\* S-50 MIDI IMPLEMENTATION \*\*\*

Version 1.00  
Aug. 25 1986

## 1. TRANSMITTED DATA

Status	Second	Third	Description
1001 nnnn	0kkk kkkk	0000 0000	Note OFF kkkkkkkk = 36 - 96
1001 nnnn	0kkk kkkk	0vvv vvvv	Note ON kkkkkkkk = 36 - 96 vvvvvvvv = 1 - 127
1011 nnnn	0000 0001	0vvv vvvv	Modulation vvvvvvvv = 0 (OFF) vvvvvvvv = 127 (ON)
1011 nnnn	0000 0111	0vvv vvvv	Volume vvvvvvvv = 0 - 127
1011 nnnn	0100 0000	0111 1111	Hold1 ON
1011 nnnn	0100 0000	0000 0000	Hold1 OFF
1100 nnnn	0ppp pppp		Program Change pppppppp = 0 - 127
1101 nnnn	0vvv vvvv		Channel After Touch vvvvvvvv = 0 - 127
1110 nnnn	0vvv vvvv	0vvv vvvv	Pitch Bend Change
1011 nnnn	0111 1011	0000 0000	ALL NOTES OFF
1011 nnnn	0111 1100	0000 0000	OMNI OFF
1011 nnnn	0111 1111	0000 0000	POLY ON

## 2. RECOGNIZED RECEIVE DATA

Status	Second	Third	Description
1000 nnnn	0kkk kkkk	0vvv vvvv	Note OFF, velocity ignored
1001 nnnn	0kkk kkkk	0000 0000	Note OFF kkkkkkkk = 0 - 127
1001 nnnn	0kkk kkkk	0vvv vvvv	Note ON kkkkkkkk = 0 - 127 vvvvvvvv = 1 - 127
1011 nnnn	0000 0001	0vvv vvvv	Modulation vvvvvvvv = 0 - 127
1011 nnnn	0000 0111	0vvv vvvv	Volume vvvvvvvv = 0 - 127
1011 nnnn	0100 0000	01xx xxxx	Hold1 ON
1011 nnnn	0100 0000	00xx xxxx	Hold1 OFF
1100 nnnn	0ppp pppp		Program Change pppppppp = 0 - 127
1101 nnnn	0vvv vvvv		Channel After Touch vvvvvvvv = 0 - 127
1110 nnnn	0vvv vvvv	0vvv vvvv	Pitch Bend Change
1011 nnnn	0111 1011	0000 0000	ALL NOTES OFF
1011 nnnn	0111 1100	0000 0000	OMNI OFF
1011 nnnn	0111 1101	0000 0000	OMNI ON
1011 nnnn	0111 1110	0000 0000	(MONO ON)
1011 nnnn	0111 1111	0000 0000	POLY ON

## Notes :

\*1 Received if the corresponding function switch is ON.

## Notes :

\*1 Transmitted if the corresponding function switch is ON.

\*2 Transmitted when 'Patch Number' is changed. Program number (ppppppp) corresponding to a Patch can be set freely.

\*3 When the 'Patch Number' is changed, this message is sent.

\*4 When power is first applied, these messages are transmitted.

\*2 Recognized when appropriate program number corresponding to a Patch is received.

\*3 Mode Messages (123 - 127) are also recognized as ALL NOTES OFF.

\*4 MONO ON message is ignored.

**MIDI IMPLEMENTATION CHART**

		Date : Aug. 25 1986	
Model	S-50	MIDI Implementation Chart	Version : 1.00
Function ...		Transmitted	Recognized
Basic	Default	1 - 16	1 - 16
Channel	Changed	1 - 16	1 - 16
Mode	Default	Mode 3	Mode 1, 3
Messages	*1	Mode 3	POLY, OMNI ON/OFF
	Altered	*****	MONO ignored
Note	36 - 96	0 - 127	
Number	True voice	*****	0 - 127
Velocity	Note ON	o	*1
	Note OFF	x	9n v = 0
After	Key's	x	x
Touch	Ch's	*1	*1
Pitch Bender		*1	*1 0 - 12 seml 9 bit resolution
	1	*1	*1 Modulation
	7	*1	*1 Volume
	64	*1	*1 Hold1
Control			
Change			
Prog		*1 0 - 127	*1 0 - 127
Change	True #	*****	0 - 127
System Exclusive		x	x
System	Song Pos	x	x
	Song Sel	x	x
Common	Tune	x	x
System	Clock	x	x
Real Time	Commands	x	x
Aux	Local ON/OFF	x	x
	All Notes OFF	o (123)	o (123-127)
Mes-	Active Sense	x	x
sages	Reset	x	x
Notes		*1 Can be set to o or x manually, and memorized by disk.	
		*2 Memorized by disk.	
		*3 Program change numbers for each Patch can be set freely.	
Mode 1 : OMNI ON, POLY	Mode 2 : OMNI ON, MONO	o : Yes	
Mode 3 : OMNI OFF, POLY	Mode 4 : OMNI OFF, MONO	x : No	

**MEMO**